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***Abstract*—The state-of-the art RF and millimeter-wave first-cut circuits design requires simple hand calculation methods to avoid time-consuming iterative simulations. The classical MOSFET sizing methods used in advanced technologies, still rely on questionable and inaccurate concepts. Moreover, the pessimistic rules of thumb proposed for older bulk technologies are no more useful and lead to overdesign. This work takes advantage of the Moderate Inversion and uses low and high frequency figures of merit to provide a convenient sizing method for a 35 GHz Low Noise Amplifier (LNA) in 28 nm UTBB FDSOI technology.**

Keywords—Transconductance efficiency; gm over Id; Double-gate FETs; FDSOI; UTBB; Analog, RF; Low-Power; Low-Voltage; mm-Wave; LNA

I. INTRODUCTION

More and more wireless devices and IoT building blocks rely on CMOS analog and RF circuits to efficiently interact with the physical world. Thanks to the geometry down-scaling, CMOS MOSFETs have been widely used in low-cost and low-power RF integrated circuits (RFIC). Short-channel related issues, as side effects of the geometry shrink, have been controlled using new architectures and new materials [1][2]. The new architectures allow for excellent electrostatic control [3].

Clearly the UTBB FDSOI technology has proven to be suitable for Analog and RF applications, especially when both power consumption and performance are valued equally. UTBB FDSOI MOSFETs exhibit high analog and RF performances thanks to the reduced parasitic capacitances and resistances [4]. Moreover, the independent back gate provides an interesting degree of freedom that allows tradeoff between power consumption and performance [5][6].

Several circuit-topology-based techniques such as current reuse are proposed in analog design to optimize performance and power consumption [7]. These techniques are out of this paper scope. In this work, the UTBB FDSOI characteristics are used for first-cut analog sizing method. In particular, the transconductance efficiency versus inversion coefficient (IC) studied in [6] is used to determine the width of the MOSFET while the transit frequency (f_T) versus IC charts are used for length selection. The design method, using relaxed length and Moderate Inversion (MI) regime, provides a valuable tradeoff between gain, power consumption and performance while MOSFET width is kept reasonably large and short channel effects are mitigated. An eye is also kept on passive devices limitations from the very beginning of the sizing flow.

This paper is organized as follows. First, the classical analog design methods, based on inherited rules of thumb, are briefly discussed in Section II. Second, the UTBB FDSOI technology capabilities for Analog and RF applications are reminded in Section III. Third, the transconductance (g_m) over drain current (I_D) based design method is presented in Section IV. Fourth, the high frequency performance versus IC and MOSFET length is assessed in Section V. Finally, a 35 GHz LNA design tradeoff in Moderate Inversion is proposed in Section VI and a conclusion is given in Section VII.

II. CLASSICAL DESIGN SIZING METHODS IN ANALOG AND RF

Sizing MOSFETs through iterative simulations and trial and error practices takes considerable amount of the precious design time. Optimum design tradeoff is hardly achieved using these methods [8]. Furthermore, hand calculation based analog design remains the method of choice to minimize iterative simulations and enables intuitive design. The classical hand calculation sizing methods are still based on inaccurate and questionable concepts such as the gate voltage overdrive ($V_{ov} = V_{GS} - V_{TH}$, where V_{TH} is the threshold voltage), and pessimistic rules of thumb such as the shortest possible length for higher f_T, higher V_{ov} constraint, and a maximum operation frequency of $f_T/10$.

Design in Moderate Inversion has become attractive in advanced technologies as it offers the optimum trade-off between speed, transconductance, and power consumption [9][10]. However, the classical gate voltage overdrive is becoming a poor metric for MOSFET inversion level assessment in advanced technologies as it is based on conflicting definitions of the threshold voltage [11]. The latter is defined as the V_{GS} value at the onset of the Strong Inversion (SI) and extracted using several methods and criteria leading to uncorrelated definitions. Moreover, gate overdrive voltage can only be used for the hand calculation sizing method based on SI square law that miserably fails to predict g_m/I_D in MI as seen in Fig. 1. Even for a long channel device, the error is more than 100% at V_{ov} = 100 mV. For short channel devices (e.g. L = 30 nm in Fig. 1), the simple square law is not valid in all levels of inversion. Moreover, for a double gate transistor such as the

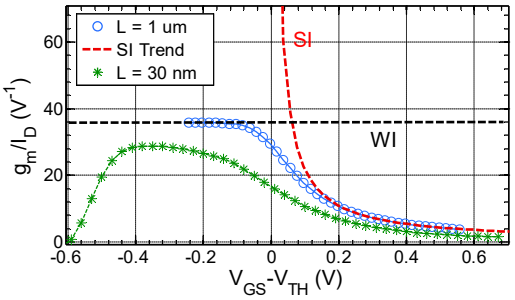

Fig. 1 Square law model (SI) and weak inversion exponential model failures to predict measured g_m/I_D in MI for a long and short channel devices. V_{TH} is defined here as the V_{GS} at the maximum of $\partial C_{gc}/\partial V_{GS}$.

UTBB FDSOI MOSFET, we experimentally observe two separate threshold voltages in the forward back gate bias condition while considering the C-V and its derivative both shown respectively in Fig. 2 and its Inset. Consequently, the gate overdrive voltage becomes impractical for describing the level of inversion of the advanced MOSFET architectures. It should be noted that V_{ov} can become negative in MI and for lower levels of inversion, and thus becomes useless.

In RF circuits, designers tend to use shortest devices to get highest possible transit frequency f_T and consequently better performance. However, shortest MOSFETs are subject to detrimental short channel effects, lower intrinsic voltage gain, and higher mismatch. In Fig. 3, Drain-Induced-Barrier-Lowering (DIBL) versus the gate length is shown for bulk and FDSOI technologies. Using relaxed and non-minimal lengths provides lower DIBL effect and lower variability while frequency performance is still high enough for the majority of today's applications in the RF spectrum as shown in **Erreur ! Source du renvoi introuvable.** where f_T is plotted versus the Inversion Coefficient (IC) for various MOSFET lengths in 28 nm UTBB FDSOI technology. IC is defined as:

$$IC = \frac{I_D}{I_\square \cdot \left(\frac{W}{L}\right)} \qquad (1)$$

where I_D, W and L are respectively the drain current, the width, and the length. $I_\square$ is the square current at the middle of the moderate inversion with a value of about 0.7 µA for 28 nm UTBB FDSOI [6]. For L = 100 nm, the maximum transit frequency is still in the mm-Wave spectrum (> 100 GHz) for the FDSOI technology while DIBL is reduced by 23mV/V with respect to L = 28 nm. Moreover, according to (1) and for fixed I_D and inversion level IC, the device area increases as L^2, which is beneficial for local mismatch effect.

Normalized module and phase of the transadmittance Y_{21} are respectively shown in **Erreur ! Source du renvoi introuvable.** and **Erreur ! Source du renvoi introuvable.** versus frequency for different lengths and at V_{GS} = 0.5 V. The transadmittance is normalized using $I_\square/U_T$ where U_T is the thermal voltage. All devices are operating in the MI regime. At V_{GS} = 0.5 V, shorter channels (L < 100 nm) are biased at an inversion coefficient of 6.3, while for L = 100 nm, IC = 5.1. For L = 100 nm and at IC = 5.1, with a transit frequency f_T of 70 GHz, the $f_T/10$ rule of thumb gives, 7 GHz. At this limit frequency no degradation on the Y_{21} module is observed and a phase shift of less than 4° is

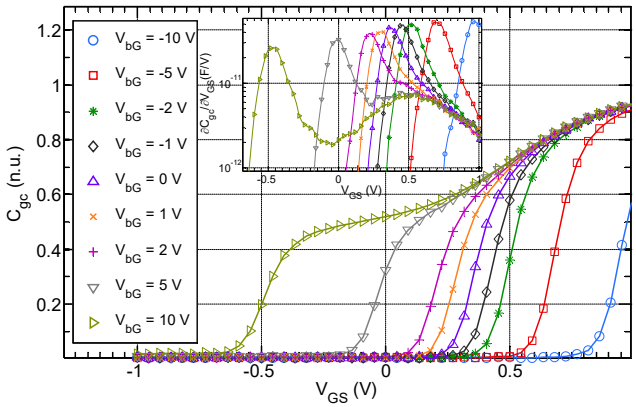

Fig. 2 Measured gate to channel capacitance normalized using front oxide capacitance (C_{ox}.W.L) with respect to V_{GS} for various V_{bG} and its derivative (Inset) for N-type UTBB FDSOI MOSFET.

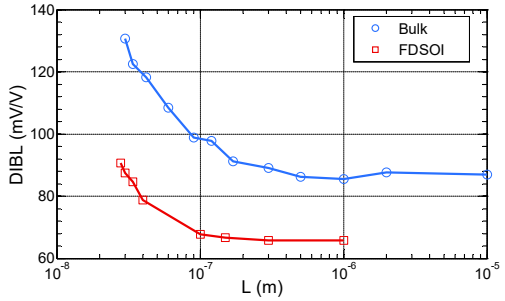

Fig. 3 Comparison of DIBL between FDSOI and Bulk in saturation (V_{DS}=1V) and V_{bG} = 0 V.

measured. The finger length of the measured structures is 1 µm and the lateral gate distributed effect is largely contributing to the measured phase shift. Though, a phase shift of 10° is measured at 19 GHz with no degradation on $|Y_{21}|$. In summary, it is clearly evidenced that non minimal channel lengths (i.e. L> 30nm in 28 nm node) in advanced technologies provide high enough f_T values that can still be used to design RF circuits, while the conservative $f_T/10$ rule of thumb is misleading, in particular at low inversion levels. 'Common' rules are then inaccurate and lead to overdesign. To overcome these issues, optimal geometries and bias conditions are approximated using time-consuming iterative numerical simulations. Other sizing methods based on the Inversion Coefficient concept have been proposed [12]. However, in many circuits where passive elements play a key role such as Low Noise Amplifier (LNA), circuits are optimized using time-consuming iterations of the IC based method since no passive part related constraints are considered in the active part optimization [13].

III. ADVANTAGES OF UTBB FDSOI TECHNOLOGY

In the UTBB FDSOI technology, MOSFET channel is formed in a thin silicon film separated from the substrate by an oxide film called the Buried OXide (BOX). In 28 nm FDSOI technology, the final silicon film is 7nm thick after process [2]. This architecture provides with multiple advantages for high performance and low power applications. In the addition of the well-known SOI technology advantages [14][15], UTBB

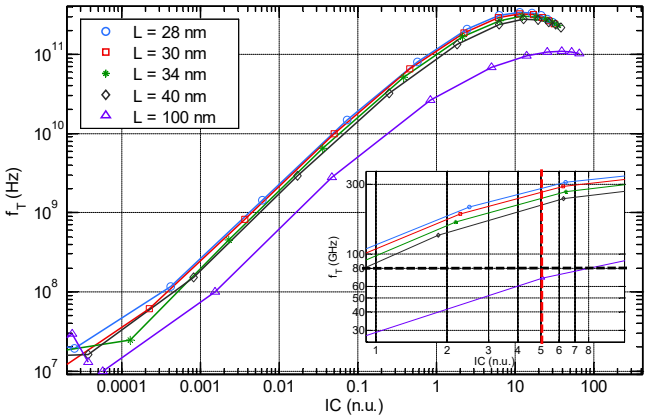

Fig. 4 Measured f_T versus IC for various MOSFET lengths in saturation (V_{DS}=1V). Inset gives a focus on the second part of the MI (1 < IC < 10)

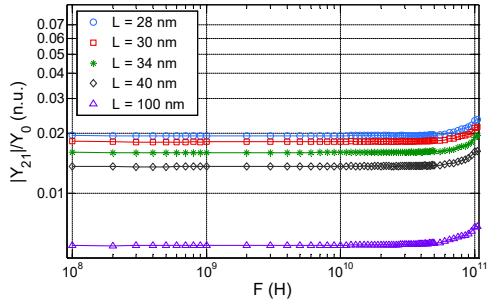

Fig. 5 Measured and normalized $|Y_{21}|$ versus frequency for various lengths and finger length is 1 µm.

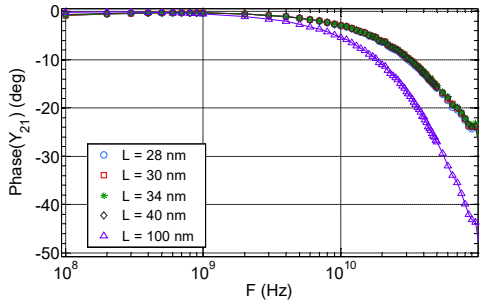

Fig. 6 Phase shift of the transadmittance Y_{21} versus frequency for various lengths and finger width W_f = 1 µm.

FDSOI technology features lower parasitic capacitances and then high-speed operation. The harmful parasitic substrate coupling is avoided in the UTBB FDSOI by introducing the Ground Plane (GP) which is a highly doped region underneath the thin BOX [16]. The ground-plane implantation under the BOX is well-type in the structures studied in this work. FDSOI technology allows co-integration of both bulk and SOI devices on the same die thanks to BOX opening for the bulk parts with a dedicated mask [17].

With less parasitic capacitances, supply voltage can be lowered for reduced power consumption with still high speed operation. Other advantages of UTBB FDSOI are steep subthreshold slope [8], reduced SCE (cf. Fig. 3), tolerance to radiation as for standard SOI and high temperatures, even though buried oxide isolation is known to give birth to temperature increase because of self-heating effect [17]. However, thanks to a thinner BOX in the UTBB FDSOI, thermal effects influence on device parameters are limited in comparison with standard SOI [18].

The advantages of the UTBB FDSOI technology make it possible to implement high performance MOSFETs operating at a low voltage, specifically in the moderate inversion regime. An understanding of the fundamental behavior of the UTBB FDSOI MOSFETs at high frequency is essential for circuit design and a sizing method in MI is a must.

IV. G_M OVER I_D INVARIANCE BASED METHOD

In digital CMOS circuits, static power consumption is mainly related to the leakage current. However, in analog circuits, biasing current is the main contributor for circuit power consumption. Thus, the devices used in analog blocks need to be permanently biased in the appropriate region. Besides power supply voltage lowering in recent technology nodes, the current budget should be reduced as well.

In RF circuits, a good tradeoff between speed and low current budget is satisfied in moderate inversion. However, for advanced devices such as the asymmetric double gate MOSFETs, the validity of classical hand calculation expressions is questionable. The lack for simple expressions for hand calculation can be reasonably contained using measurement based charts. The measured transconductance efficiency charts assessed in [6], can be used to size the transistor and to ensure its operation in moderate inversion. The invariance of the g_m over I_D chart in MI for L ≥ 100 nm makes is easy to generate the required chart. If we take into account the slope degradation using the slope factor n_1, shorter geometries can also be accounted for with same merged chart. In **Erreur ! Source du renvoi introuvable.**, g_m over I_D charts are shown versus IC. A longer geometry (L = 1 µm) is also shown for comparison. Using these charts, the g_m over I_D value can be reasonably retrieved for any selected IC and for each displayed geometry from WI to SI.

Recently, it is claimed that preselecting drain current (I_D), IC, and channel length is the most efficient way to size MOSFETs in analog circuits [12]. However, the proposed simple expressions of MOS performance mainly rely on EKV formalism which has been extrapolated to a symmetric DG in [18] but not yet transposed to the asymmetric DG. However, the choice of the inversion coefficient as a measure of the inversion level in the channel happens to be totally justified since it accurately describes the inversion charge and consequently the operating regime for single or double gate MOSFETs [12][6]. According to **Erreur ! Source du renvoi introuvable.**, selecting an IC value is equivalent to setting g_m over I_D of the device. Moreover, based on (1), once IC an I_D are known, the geometry ratio (W/L) can be calculated.

V. HIGH FREQUENCY PERFORMANCE ASSESSMENT

One of the interesting high frequency FoM is the transit frequency f_T that estimates the high frequency amplification limit and also provides an insight of the transconductance to input capacitance ratio ($f_T \approx g_m/C_{gg}$) of the MOSFET. The transit frequency versus IC charts for several lengths provide

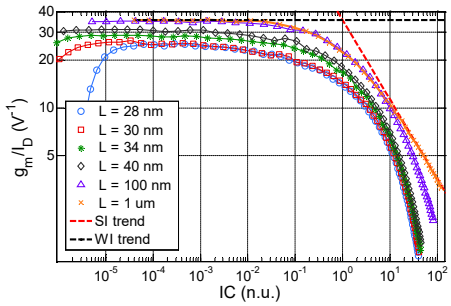

Fig. 7 g_m over I_D charts versus IC for several short NMOS along with a longer channel (L = 1 µm) for comparison.

high frequency performance limits since f_T represents the frequency at which current gain falls to unity. However, it should be noted that the transistor can operate at any frequency even beyond this limit, provided that non-quasi-static related limitations are carefully taken into account and modeled. The module and phase of the transadmittance versus frequency charts (e.g. **Erreur ! Source du renvoi introuvable.** and **Erreur ! Source du renvoi introuvable.**) can also be used to estimate the phase shift and module drop when frequency is set beyond f_T. As stated in Section II, the rule of thumb stating that maximum frequency of operation must be lower than $f_T/10$ is too stringent. This rule of thumb finds its origin in the validity of the quasi-static model proposed in [19] and thus is essentially a misinterpretation.

VI. LNA DESIGN USING MI TRADEOFF IN UTBB FDSOI

In this Section, the focus will be on another challenge which is the transistor sizing. The RF designer dilemma is to calculate transistor geometry and current in order to get maximum amplification, minimum degradation of the signal-to-noise ratio, and minimum power consumption. The goal is to provide an illustration of a design method mainly based on the charts and properties described in Section IV and V.

One of the key building blocks in a wireless system is a Low Noise Amplifier (LNA). The LNA circuit amplifies the input signal with minimum degradation of the signal-to-noise ratio. One of the challenges RF designers must face is the simultaneous matching of the noise and the input impedance for the same source impedance. This challenge is beyond the scope of this paper therefore ideal impedance matching is considered here. However, a constraint on the value of the inductors is considered in order to account for integrated inductors with acceptable quality factors.

One of the most used circuit topologies for an LNA is the narrowband cascode. The cascode transistor is used to isolate the input from the inductive load. In particular, the Miller effect is reduced for the input transistor. However, using a cascode topology leads to a minimal room for drain to source voltage required to set both transistors in saturation. This also corroborates the need for MI operation as V_{DSAT} is lower in this regime. The circuit of the cascode LNA is shown in Fig. 8. The transistor M_1 is the input transistor and M_2 is the cascode transistor. Both transistors are chosen to have same geometry. Degeneration inductor L_s and input series inductor L_g are used for input impedance matching.

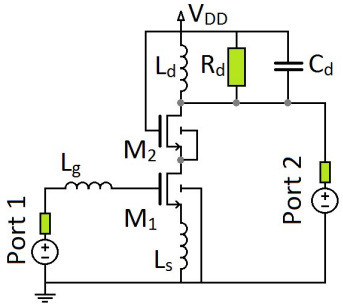

Fig. 8 LNA cascode circuit.

The following specifications are taken as an example: Drain current is 2 mA, power gain is greater than or equal to 8, operation frequency is F_0 = 35 GHz, minimal noise figure NFmin is no more than 2 dB, and input impedance is matched for 50 ohm. In order to size the circuit components and meet the aforementioned specifications, the following 3 steps are followed:

A. IC selection

The maximum value of the FoM given in (2) and representing the trade-off between high frequency performance, power consumption, and noise figure is located in the second half of the MI for short channels as shown in **Erreur ! Source du renvoi introuvable.** for two channel lengths (L = 30 nm and 1 µm).

$$FOM = \frac{g_m}{I_D} \cdot \frac{f_T}{NF_{min}} \qquad (2)$$

Optimal IC lays, at least theoretically, between IC = 4 and IC=10. Depending of the length selection, corresponding IC will be chosen where FOM is maximum.

B. Passives related constraints and Length selection

In order to avoid passive components with degraded quality factors Q, some constraints are considered prior to MOSFETs sizing. The values are chosen within the integrated mm-Wave inductor values [25 pH – 100 pH] as in [20]. The real part of the LNA input impedance is mainly tuned using degeneration inductor L_s. The expression of this real part is given in (3), provided that M_1 intrinsic conductance influence on input impedance is neglected:

$$Re[Z_{in}] = \frac{g_m L_s}{C_{gs}} \approx 2\pi f_{Ti} L_s \qquad (3)$$

where C_{gs}, and f_{Ti} are the gate-source, and intrinsic transit frequency of M_1, respectively. The specification related to impedance matching fixes the real part of Z_{in} at 50 ohm and consequently a relation between the inductance L_s and the transit frequency is given by (3). If we consider a maximum L_s inductance of 100 pH, M_1 transit frequency f_{Ti} should be greater than 80 GHz. According to Inset of **Erreur ! Source du renvoi introuvable.**, for operation at IC = 4, the MOSFET length that guarantees the required f_T is strictly greater than L = 100 nm. To obtain acceptable noise figures and using NF_{min} versus IC charts (not shown here), length should also be lower than 100 nm. In order to verify the noise figure specification and inductor value

constraint, we will consider two channel lengths that are L = 40 nm and L = 70 nm, with

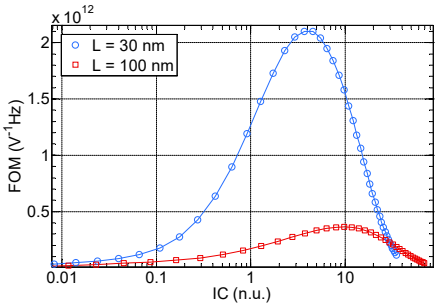

Fig. 9 FOM versus IC for two lengths.

FOM maximizing respectively at IC = 5 and IC = 9. Both geometries provide acceptable high frequency performance. Moreover, L = 40 nm and L = 70 nm MOSFETs are less subject to DIBL and Mismatch than minimal length. Thus, an L_s value of 33 pH and 39 pH for respectively L = 40 nm, and L= 70 nm MOSFET based LNAs are found.

The LNA is designed to operate at F_0 = 35 GHz and consequently, to cancel the input impedance imaginary part at this resonance frequency, the inductor L_g is tuned with a target value given by [21]:

$$L_g = \frac{1}{(2\pi F_0)^2 \cdot C_{in}} - L_s \qquad (4)$$

where C_{in} is including the total M_1 gate capacitance C_{gg} and the Miller effect of the gate-drain capacitance (C_{gd}).

C. *Width and V_{GS} calculations*

The Width is calculated using the following expression:

$$W = \frac{I_D}{IC \cdot I_\square} \cdot L \qquad (5)$$

Close width values of 22.8 µm and 22.1 µm are found for respectively L = 40 nm and L = 70 nm based LNA circuits.

The gate voltage overdrive with respect to IC charts (not shown here) are used to retrieve the gate to source voltage corresponding to the two IC values for each length. The calculated V_{GS} values are respectively 0.49 V and 0.55 V.

The results of the above sizing are shown in Fig. 10 versus frequency and summarized in Table 1 for the operation frequency F_0 = 35 GHz.

Table 1 Summary of the two LNAs parameters at F_0 = 35 GHz.

	S_{21}	S_{11}	NFmin
LNA (L = 40 nm)	10.9	-31	1.5
LNA (L = 70 nm)	8.6	-21.5	2

Power gain is lower for the L = 70 nm based LNA because of the higher IC and consequently lower transconductance efficiency. The input impedance matching is acceptable for both LNA circuits. The NFmin value is higher for the longer channel based LNA as expected, however this can be lowered using optimized layout. The power consumption of both LNAs is 2 mW which is excellent for low-power applications.

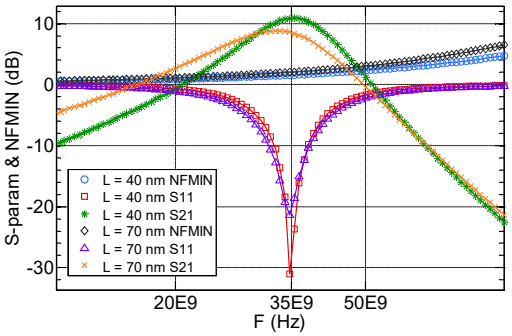

Fig. 10 Power gain S21, Input Match S11, and minimal noise figure NFmin with respect to frequency for two LNA circuits (first with MOSFET length of 40 nm and second with 70 nm).

VII. Conclusion

In this work, a constrained sizing methodology is proposed for the UTBB FDSOI MOSFET. The methodology is based on f_T versus IC measured or simulated curves for the length selection, and on g_m over I_D charts for the width calculation. The Inversion Coefficient is fixed to a value where the MOSFET optimum performance is expected, making this analysis dependent only on the channel current, and 'independent' of the front and back gate biases, a great simplification in terms of analysis. The methodology takes into account the passive components limitations and thus requires less if not minimal iterations.

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