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Multicore Systems On-Chip: Practical Software/Hardware Design

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To my wife Sonia,
my kids Tesnim and Beyram,
and my parents.

Preface

To meet high computational demands posed by latest consumer electronic devices (PDAs, cell phones, laptops, cameras, etc.), current systems employ a multitude of multicore on a single chip. The attraction of multicore processing for power reduction is compelling. By splitting a set of tasks among multiple processor cores, we can reduce the operating frequency necessary for each core, allowing to reduce the voltage on each core. Because dynamic power is proportional to the frequency and to the square of the voltage, we get a big gain, even though we may have more cores running. Even static power improves as we turn down supply voltage. However, there are several barriers to designing general purpose and embedded multicore systems. Software development becomes far more complex due to the difficulties in breaking a single processing task into multiple parts that can be processed separately and then reassembled later. This reflects the fact that certain processor jobs cannot be easily parallelized to run concurrently on multiple processing cores and that load balancing between processing cores – especially heterogeneous cores – is very difficult. The other set of problems with multicore systems design are hardware-based.

The book consists of seven chapters. The first chapter introduces multicore system architecture and describes a design methodology for these systems. The architectures used in conventional methods of MCSoCs design and custom multiprocessor architectures are not flexible enough to meet the requirements of different application domains and not scalable enough to meet different computation needs and different complexities of various applications. This chapter will emphasize on the design techniques and methodologies

Power dissipation continues to be a primary design constraint in single and multicore systems. Increasing power consumption not only results in increasing energy costs, but also results in high die temperatures that affect chip reliability, performance, and packaging cost. Energy conservation has been largely considered in the hardware design in general and also in embedded multicore system' components, such as CPUs, disks, displays, memories, and so on. Significant additional power savings can be also achieved by incorporating low-power methods into the design of network protocols used for data communication (audio, video, etc.). Chapter two investigates in details power reduction techniques at components and the network protocol levels.

Conventional on-chip communication design mostly use *ad-hoc* approaches that fail to

meet the challenges posed by the next-generation Multicore Systems-on-Chip (MCSoC) designs. These major challenges include wiring delay, predictability, diverse interconnection architectures, and power dissipation.
A Network-on-Chip (NoC) paradigm is emerging as the solution for the problems of interconnecting dozens of cores into a single system-on-chip. However, there are many problems associated with the design of such systems. These problems arise from non-scalable global wire delays, failure to achieve global synchronization, and difficulties associated with non-scalable bus-based functional interconnects.
In chapter three, we explain low-power and low-cost on-chip architectures in terms of router architecture, network topology, and routing for multi- and many-core systems.

To overcome challenges from high power densities and thermal hot spots in microprocessors, multi core computing platforms have emerged as the ubiquitous computing platform from servers to embedded systems. But, providing multiple cores does not directly translate into increased performance for most applications.
With the rise of multi-core systems and many-core processors, concurrency becomes a major issue in the daily life of a programmer. Thus, compiler and software development tools will be critical to help programmers create high performance software. Chapter four covers software issues of a so-called parallelizing queue compiler targeted for future single and multicore embedded systems.

Chapter five presents practical hardware design issues of a novel dual-execution mode processor (DEP) architecture targeted for embedded applications. Practical hardware design results and advanced optimization techniques are presented in a fair mount of details

Chapter six presents design and architecture of a produced order Queue core based on Queue computing and suitable for low power computing.

With the proliferation of portable devices, new multimedia-centric applications are continuously emerging on the consumer market. These applications are pushing computer architecture to its limit considering their demanding workloads. In addition, these workloads tend to vary significantly at run time as they are driven by a number of factors such as network conditions, application content, and user interactivity. Most current hardware and software approaches are unable to deliver executable codes and architectures to meet these requirements. There is a strong need for performance-driven adaptive techniques to accommodate these highly dynamic workloads. Chapter seven shows the potential of these techniques in both software and hardware domains by reviewing early attempts in dynamic binary translation on the software side and FPGA-based reconfigurable architectures on the hardware side. It puts forward a preliminary vision for unifying runtime adaptive techniques in hardware and software to tackle the demands of these new applications. This vision will not be possible to realize unless the notorious reconfiguration bottleneck familiar in FPGAs is addressed.

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