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Image Acquisition and Storage System of Binocular Camera Based on FPGA

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Abstract. In order to better solve the problem that image processing technology is strict in real-time and stability, a binocular camera image acquisition and storage system based on FPGA is designed with the advantage of FPGA parallel processing. The system uses Xilinx ARTIX-7 XC7A35T as the master chip to control the CMOS camera as the image sensor for image acquisition, stores the acquired images in DDR3 SDRAM, and displays the images in the host computer by reading the memory data. The results show that the system has good real-time performance and stability, and meets the requirements of image transmission and processing.

Keywords. image processing, FPGA, verilog

1. Introduction

Approximately 70% of the information that humans obtain comes from vision, which uses image sensors to acquire visual images, and uses machine vision instead of humans to perceive and explore the environment by processing the acquired images and obtaining more information[1]. With the development of technology, vision technology is widely used in all areas of society. With the increasingly stringent requirements for real-time image processing in applications, the speed of image acquisition has greatly affected the development of image processing technology[2].

FPGAs overcome the shortcomings of custom circuitry and solve the problem of fewer gates for other programmable devices[3]. Moreover, FPGAs are rich in wiring resources, reprogrammable and affordable, so they are widely used in digital circuit design. The FPGA is used to control the image sensor to acquire the image information of the target and to process the directly acquired image to meet the requirements of real-time and stability of image processing[4]. By using FPGA to control sensors for real-time acquisition of targets, the effectiveness and stability of the system can help obtain more effective information. The application of real-time image acquisition and storage technology is increasingly widespread. The experimental results show that the whole system has low cost, loose shooting conditions, stable imaging in multiple scenes, and high imaging accuracy[5].

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2. Real-time FPGA-based Binocular Camera Image Acquisition System

2.1. Overall System Design

The overall workflow of the system is as follows: the FPGA master control process configures the image sensor through the driver of the IIC, writes the captured image from the sensor to the DDR control module, the DDR control module saves the data to the DDR3 SDRAM, and the HDMI top-level module reads the captured image data from the DDR3 and drives the display to show the image. Overall structure diagram of the system is shown in Figure 1.

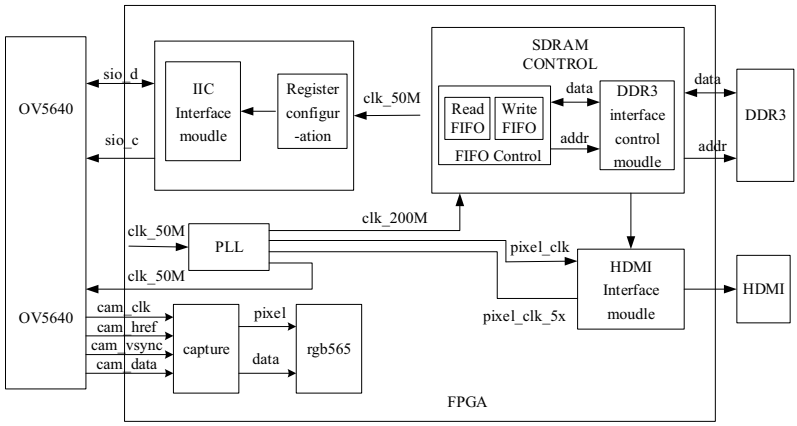

Figure 1. structure of system

In the FPGA-based binocular camera image real-time acquisition system, it mainly contains clock module, IIC driver module, DDR3 SDRAM cache module and HDMI display module. The clock module is used to provide the driving clock for the IIC driver module, HDMI top-level module, and DDR3 control module; the IIC driver module and IIC configuration module are used to initialize the image sensor; the acquisition module is responsible for acquiring camera image data and writing the acquired data to the DDR3 control module; the DDR3 control module writes and reads user data to and from the off-chip DDR3 memory; the HDMI module is responsible for driving the HDMI display.

2.2. Hardware Selection

The FPGA host chip used is Xilinx's ARTIX-7 series FPGA chip, model XC7A35T . The main parameters of the FPGA chip XC7A35T are shown in the table 1.

Table 1. XC7A35T Parameter Table

Name	Parameters
Slices	5,200
CLB flip-flops	41,600
Logic Cells	33,280
Block RAM (kb)	1,800

The DDR3 SDRAM memory uses Micron's 2Gbit DDR3 chip, model MT41J128M16HA-125, which has a total DDR bus width of 16 bits and operates at a maximum clock speed of 400MHz.

3. Hardware and Driver Design

3.1. Image Acquisition Module

The image sensor used in the image acquisition module is the ov5640 camera. Before the OV5640 works properly, it is configured to work in the desired mode by configuring the registers. Since the images captured by the camera will eventually be displayed via HDMI, the pixel data output from the OV5640 camera is configured in RGB565 format.

The interface to the configuration registers, the SCCB interface, is compatible with the IIC protocol[6]. The interface bus consists of the SIO_C clock input lines and the SIO_D bidirectional data line, which are equivalent to the SCL and SDA signal lines of the IIC protocol, respectively. So the camera can be configured directly using the IIC driver. The image data captured by the camera is cached using the internal FIFO of the FPGA[7].The SCCB write transfer protocol is shown in Figure 2.

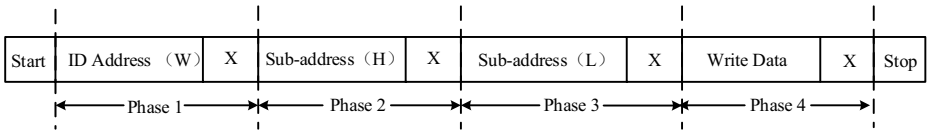

Figure 2. SCCB Write Transfer Protocol

ID ADDRESS is composed of 7-bit device address and 1-bit read/write control bit (0: write, 1: read); Sub-address(H) means high 8-bit register address, Sub-address(L) means low 8-bit register address, Write Data is 8-bit write data, each register address corresponds to 8-bit configuration data. address(H) indicates the high 8-bit register address, Sub-address(L) indicates the low 8-bit register address, Write Data is 8-bit write data, and each register address corresponds to 8-bit configuration data.

3.2. DDR3 Cache Module

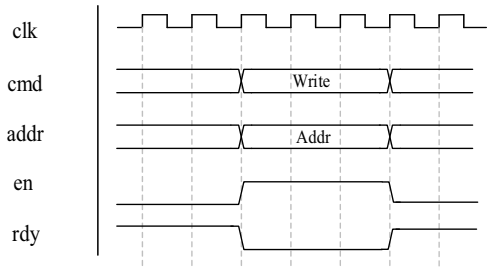

Figure 3. Write Command Timing

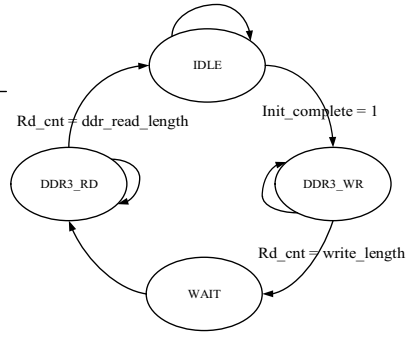

Figure 4. The state transition diagram of DDR3

DDR3 SDRAM is based on SDRAM technology[8]. Compared to SDRAM, the most important feature of DDR SDRAM is double-edge triggering, and DDR SDRAM can read and write twice as fast as traditional SDRAM with the same operating clock[9].

DDR3 reads or writes include write command operations. write command timing is shown in the figure 3. First check “rdy”, if it is high, the IP core command reception is ready to receive user commands, pull up “en” at the current clock, send command and

address at the same time, then the command and address are written. The state transition diagram of DDR3 is shown in Figure 4.

3.3. FIFO cache

The DDR3 storage module cannot be separated from the FIFO when storing data. FIFO is a first-in-first-out data register that can cache continuous data streams to prevent data loss during incoming and storage operations. After the acquisition of image data, in order to better solve the problem of cross-clock domain, FIFO should be used to cache the data. Generation of read and write FIFO IP cores is shown in Figure 5.

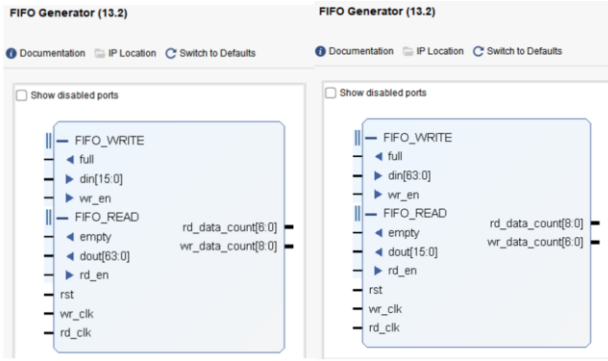

Figure 5. Read and write FIFO IP cores

Before storing the user data into the DDR3 memory, the collected data is first written to the FIFO buffer. The DDR3 control module reads data from the FIFO cache and writes it to the DDR3 memory, at which time the data in the FIFO cache is constantly decreasing. The write port of the FIFO is connected to the client, the write data comes from the client, and the read port is connected to the DDR3 module, and the data is read from the FIFO to the DDR3. The write port of the read FIFO is connected to the DDR3 module, the write data is from DDR3, and the read port is connected to the client. The user reads data from the FIFO, which is the cache data from DDR3. FIFO read and write experiment simulation is shown in Figure 6.

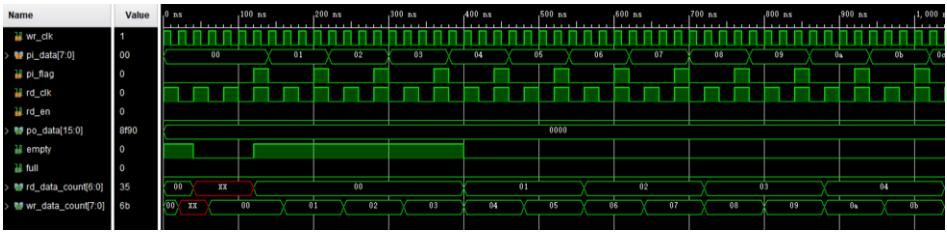

Figure 6. FIFO read and write experiment simulation

3.4. HDMI Display Module

The differential data signal and clock signal of HDMI interface are directly connected to the differential IO of FPGA, and the differential-to-parallel conversion of HMDI signal is realized inside the FPGA before decoding to realize the transmission solution of HDMI

image input[10]. The HDMI display module is responsible for driving the HDMI display while providing line and field synchronization signals and data request signals to other modules. the HDMI display module generates line and field signals, data enable signals, and horizontal and vertical coordinates of pixel points.

HDMI uses three RGB channels by default, and the fourth channel is the clock channel, which is used to transmit the pixel clock. Each pixel has a color depth of 24 bits, 8 bits for each RGB color component, so the color data on each channel is converted to a 10-bit pixel character by an encoder, as shown in Figure 7. This 10-bit character is then converted to serial data through a parallel-serial converter and finally sent out by the TMDS data channel.

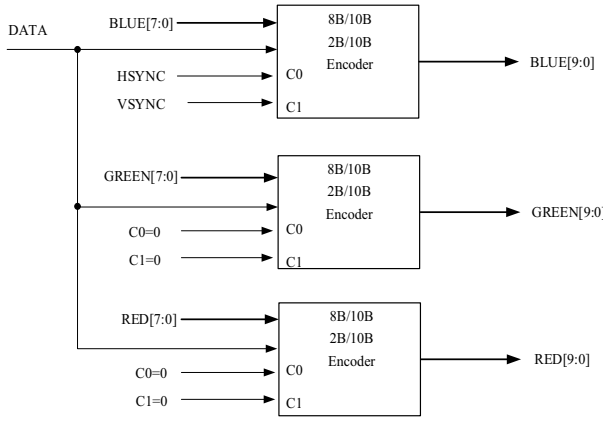

Figure 7. Schematic diagram of the encoder

4. Experimental Results

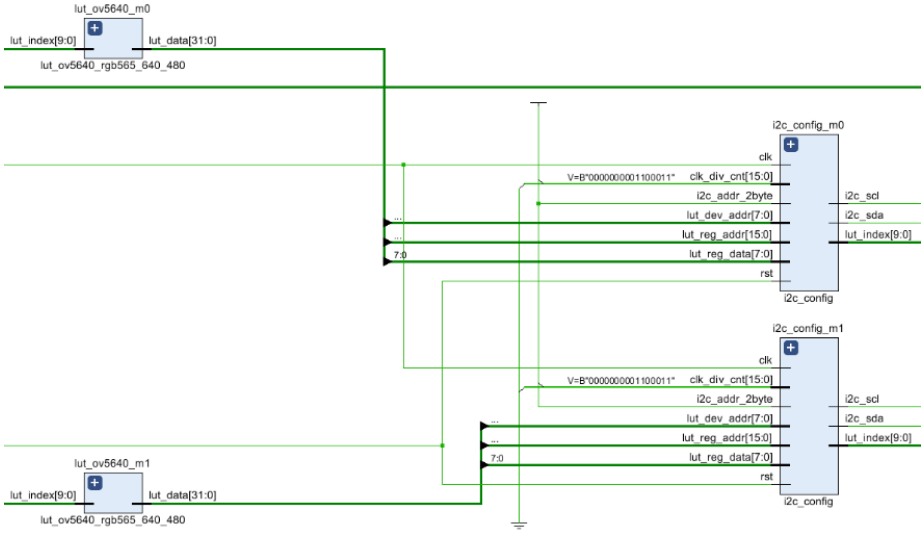

Figure 8. RTL view of the project

This experiment uses Vivado 2019.1 as the development environment. After the clock module, IIC driver module, DDR3 SDRAM cache module, and HDMI display module are designed and verified by simulation, the modules are connected through the top-level file, pin assignments are made, bitstream files are generated after compilation, and the bitstream files are downloaded to the board through the JTAG interface to drive the board. The RTL output module view is shown in Figure 8.

The whole system is verified by observing the images displayed on the host computer.

Figure 9. Graph of experimental results

The imaging effect is shown in Figure 9. The system has a good imaging effect and meets the needs of image acquisition and processing.

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