

Secure Startup Scheme for Asymmetric Embedded Software Based on Multiple Cores

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Abstract—Aiming at the real-time requirement of relay protection device, a secure startup mechanism of multi-core asymmetric software was proposed based on a self-developed chip with two clusters and four cores of ARM Cortex-A53 processor, which could meet both the security requirements of embedded devices and the real-time requirements of relay protection device. The overall design idea, security hardware protection module and software architecture of the mechanism are described, and the security is analyzed in detail. Experiments show that the proposed scheme can be used as a trusted system to measure the integrity of embedded devices, so as to realize the secure startup of embedded devices.

Keywords—Embedded system, Secure startup, Trust root, Trusted startup, Multi-core asymmetric software

1. Introduction

With the development of embedded technology, in view of the embedded intelligent terminal security has also been more and more attention. Trusted startup is the foundation of all system behavior, not only load during startup code itself, is responsible for the initialization of an embedded equipment physical device and the state of the system itself, allocate memory and hardware and software resources, etc., also start the system of service and necessary to sustain the normal operation of all kinds of process, Including secure and trusted processes. Any error during startup can cause the operation of an embedded device to enter an unpredictable and dangerous state. Trusted Computing Group (TCG) has promoted the development of trust computing technology by applying trust root and trust chain technology. Many subsequent studies are also focused on the Trusted Platform Module (TPM) of trusted computing platform [1]. Researchers from Nanrui Group have designed their own security module using OTP

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chip as trusted root for specific interface, [2] but this undoubtedly increases the burden of embedded system hardware and software system.

Therefore, ARM proposed a hardware level mobile platform security technology TrustZone [3], through the processor core unit, system bus, peripheral devices, memory, cache registers and other hardware security expansion, CPU chip is the system "trusted root". At present, embedded terminals are developing rapidly and there are many kinds. The research of this paper is based on a chip developed by ARM Cortex-A53. The software architecture of the system is also based on the strong real-time requirements of industrial systems such as power systems. The Asymmetric multi-core (AMP) structure is adopted instead of the commonly used Symmetric multi-core Symmetric Multi-Processing (SMP) [4].

2. Design and Implementation of Multi-Core Asymmetry

2.1. Security Hardware Introduction

The security hardware construction of the scheme mainly includes the following aspects:

- Core-level ARM Trustzone establishes a multi-level execution environment for trust security requirement services
- Cryptography Engines includes Crypto engines (Cipher/HASH), TRNG, Embedded DMA for transfer data between DDR and WTM, FUSE Burning Interface.
- TZC400 is used for SOC Sub-System access permission control
- Secured FUSE module for boot and system usage.
- On-chip BootROM image as the Platform Root of Trust for Secure Processors to boot up from.

2.1.1 TrustZone. TrustZone is a security architecture solution provided by ARM, which provides a secure hardware foundation for embedded systems and has been widely recognized in the industry[4]. TrustZone implements the mechanism through the hardware structure, divides the storage into safe and non-safe areas[5], and accesses it through the Cryptography Engines.[6]

2.1.2 Cryptography Engines. The Cryptography Engines unit can be instantiated either in FIPS 140-2/3 compliant mode, or in Non-FIPS (accelerator-only) mode. The FIPS mode utilizes a Hardware-Root-Of-Trust authorization scheme for authenticating the use of keys and provides the basis for secure, trusted operations. The FIPS mode contains intelligence in the form of firmware and behavior documented herein.

2.1.3 TZC400. The TZC400 operates between ACE-Lite masters and ACE-Lite slaves in a TrustZone system and filters bus accesses from masters to slaves. It performs the filtering based on security requirements that are specified for address regions. You can program the eight TZC-400 address regions with varying security requirements for your intended application. You can program the TZC-400 to report faults using the ACE-Lite response channel or interrupts. Figure 1 shows a high-level view of the TZC-400 with a control unit and between one and four filter units.

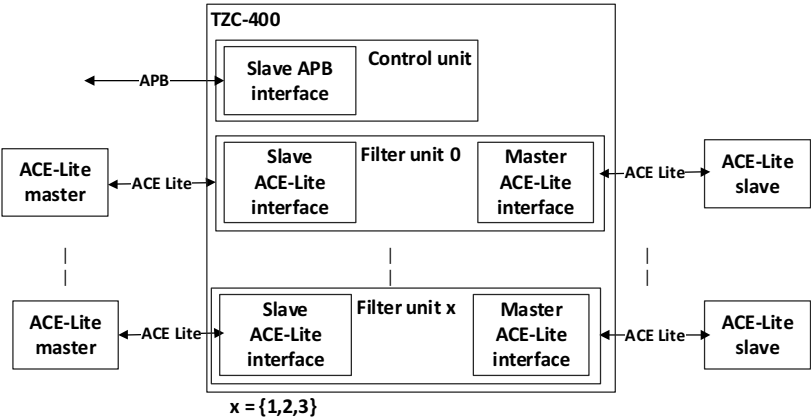


Figure 1. TZC400 overview

2.1.4 FUSE. This scheme uses TSMC HD FUSE measured in bank(256 bit) as unit, will burn one bank at every burning action, but while perform read action will update all banks' value. TSMC FUSE module has 32 bit wide data port, hardware FSM will shift all fuse value out[7]. This scheme uses double bits mode. The same data bit is stored in both fuse macro 0 and fuse macro 1. The final data is obtained by an “OR” operation of values from both macros with the same address. That means while fuse burning, for every fuse bank, we need burn twice with the same fuse value. This scheme further ensures that the data is not tampered with as shown in Figure 2

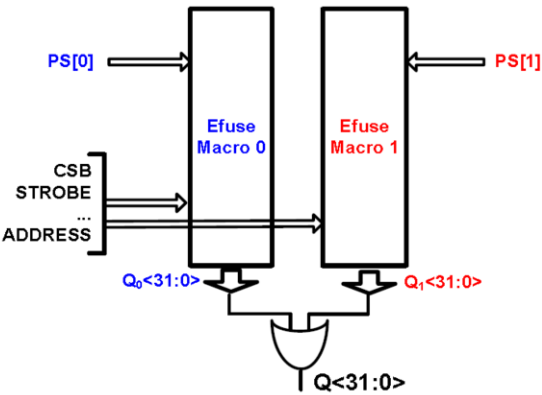


Figure 2. FUSE Dual Bit Mode

2.2. Multi-core Asymmetric Software

In order to meet the real-time requirements of the relay protection device, this paper designs the asymmetric software architecture as shown in Figure 3, and allocates hardware and memory resources for different systems in the start-up stage. linux is used to meet the requirements of multiple applications, while these strong real-time applications runs in baremetal.

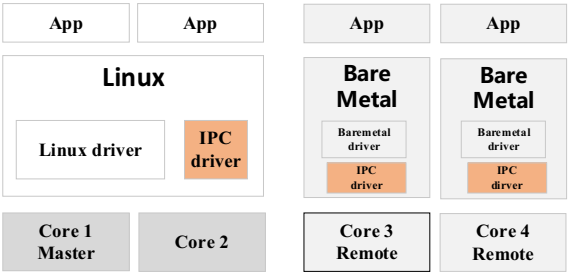


Figure 3. Asymmetric software frameworks

3. Secure Startup Design of Multi-Core Asymmetric Embedded Software

The purpose of safe startup is to ensure that the content of each stage of the system is safe during the startup process. In other words, it adopts the form of trust chain and realizes the chain transfer of trust through the integrity verification of modules at all levels. Since BootRom is written in a single time during the chip production stage, it does not allow erasable or repeated writing, which provides an absolutely trusted trust root for the chip. Core0 in Cluster0 as the master core is booted from BootRom as shown in the figure 4.

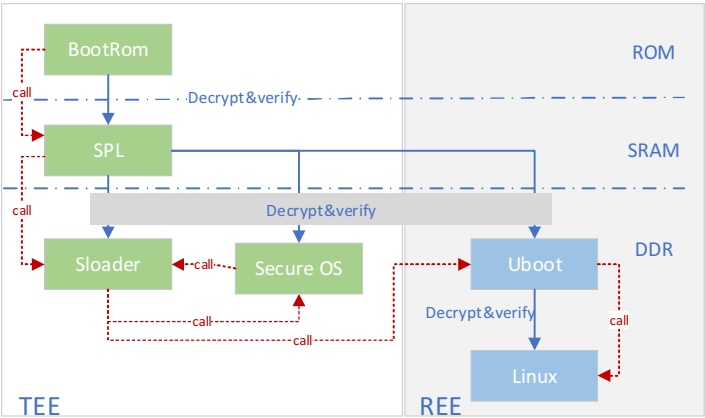


Figure 4. security start-up of master core

The BootRom starts execution from the TEE environment. SPL is loaded into SRAM by BootRom to run, the DDR is initialized, and then Sloader, Secure OS and uBOOT are loaded into the DDR. After loading, execution is transferred to Sloader. After the Secure OS is initialized by Sloader, the execution is transferred to Uboot. After entering Uboot, the system switches to the REE environment. After Uboot loads Linux into DDR, the execution transfers Linux and finally executes to the Linux Shell. The BootRom is responsible for decrypting or verifying the SPL. The SPL is responsible for decrypting or verifying the signature of Sloader, Secure OS, and Uboot. Uboot is responsible for decryption or signature verification of Linux, and the relevant decryption and signature verification process will be completed through the interface of SMC into the TEE environment (Secure OS).[8][9][10]

These ensure that the chip has an absolutely secure root of trust boot.

The real startup process is shown in Figure 5, The safe startup process of the whole system is as follows:

```
Serial-COM2104 - SecureCRT
File Edit View Options Transfer Script Tools Window Help
Enter host <Alt+R>
Serial-COM2104
emmc: bootinfo version:0x10001
BOOTROM: load spl0
BOOTROM: verify spl0... ok
SPL: Built : 10:46:12, Jan 20 2023
sys_boot_data 0x1c00
get_strappin BOOT mode.
enter spl_udl_sub mode:0
get_boot_device BOOT mode.
storage_emmc_init start
chip emmc storage.total_lba:122142720
loaded board info to 0x22d000
SPL: ddr init
i2c bus reset, send clk: 0
init 0x6160,0x10000000,0x3
init_pmic ver = 0x14
pmic buck1 = 0x98
pmic buck4 = 0xbc
ddr init begin(0)..
=== will wait status_ddr during initialization ===
mc init reg addr=[0xpi init reg addr=[0xcontroller initialized
PI initialized
ddr init end 0
*****ch0 is pass
*****ddr test pass
get_boot_device BOOT mode.
secure version update
SPL: Loading sloader.
load_addr=0x80000000,image_size=91e0
image_verify_scatter[sloader]
sloader_addr=0x80000000 sloader IMAGE size: 37344
SPL: Loading secureos.
load_addr=0x80200000,image_size=5e540
image_verify_scatter[secureos]
secureos_addr=0x80200000 secureos IMAGE size: 386368
SPL: Loading uboot.
load_addr=0xfe000000,image_size=978e0
image_verify_scatter[uboot]
uboot_addr=0xfe000000 uboot IMAGE size: 620768
SPL: at 0x80000000 spl_run_entry
NOTICE: BL31: v1.2(release):b5a4b7145
NOTICE: BL31: Built : 17:40:40 Feb 28 2023
```

Figure 5. the real startup process

In addition, as a multi-core and multi-system chip, a safe and credible trust chain not only involves the startup process of a software system, but also the safe transfer between cores is also crucial. Figure 6 shows the safe transfer and verification step by step between multiple cores, which ensures the startup safety of the whole chip [11]. When the main core is powered on and started from BootROM, other cores enter the WFE state under the guidance of SPL and wait to be loaded the code and be started.

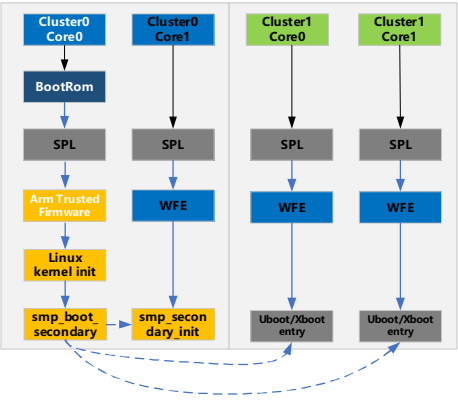


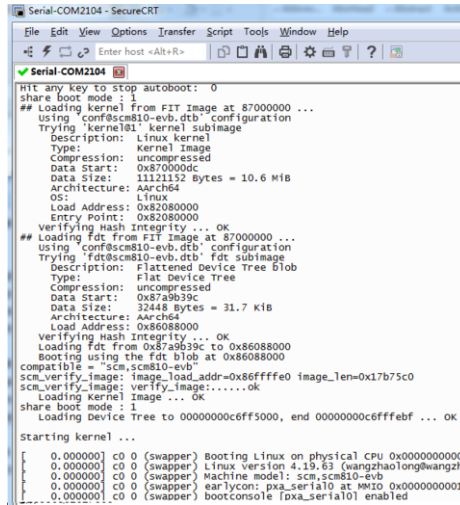
Figure 6. Multi-core security start-up framework diagram

4. Process Integrity Verification for Multi-Core Asymmetric Embedded Software

In order to verify whether the restarting mechanism can effectively resist tampering and attacks, two verification scenarios are designed here:

- Verify that when the master core firmware is modified, the startup process can be normally identified and the startup is terminated
- Verify that when the slave core firmware is modified, the boot process can correctly identify and terminate the boot of the slave core.

Verify scenario one, as shown in Figure 7, contains the correctly signed kernel image and the master core linux can boot normally.



```

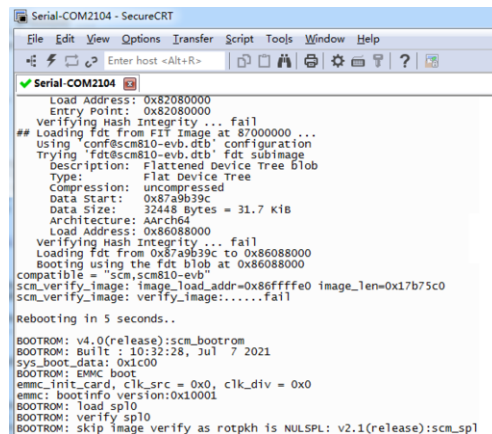
Serial-COM2104 - SecureCRT
File Edit View Options Transfer Script Tools Window Help
Enter host <Alt+R>
Serial-COM2104
Hit any key to stop autoboot: 0
share boot mode: 1
## Loading kernel from FIT Image at 87000000 ...
Using 'conf8scm810-evb.dtb' configuration
Trying 'kernel1' kernel subimage
Description: Linux kernel
Type: Kernel Image
Compression: uncompressed
Data Start: 0x870000dc
Data Size: 11121152 Bytes = 10.6 MiB
Architecture: AArch64
OS: Linux
Load Address: 0x82080000
Entry Point: 0x82080000
Verifying Hash Integrity ... OK
## Loading fdt from FIT Image at 87000000 ...
Using 'conf8scm810-evb.dtb' configuration
Trying 'fdt8scm810-evb.dtb' fdt subimage
Description: Flattened Device Tree Blob
Type: Flat Device Tree
Compression: uncompressed
Data Start: 0x87a9b39c
Data Size: 32448 Bytes = 31.7 KiB
Architecture: AArch64
Load Address: 0x86088000
Verifying Hash Integrity ... OK
Loading fdt from 0x87a9b39c to 0x86088000
Booting using the fdt blob at 0x86088000
compatible = "scm,scm810-evb"
scm_verify_image: image_load_addr=0x86ffffe0 image_len=0x17b75c0
scm_verify_image: verify_image:.....OK
Loading kernel image ... OK
share boot mode: 1
Loading Device Tree to 00000000c6ff5000, end 00000000c6ffebf ... OK
Starting kernel ...

[ 0.000000] c0 0 (swapper) Booting Linux on physical CPU 0x0000000000
[ 0.000000] c0 0 (swapper) Linux version 4.19.63 (wangzhaolong@wangzh
[ 0.000000] c0 0 (swapper) Machine model: scm,scm810-evb
[ 0.000000] c0 0 (swapper) earlycon: pxa_serial0 at MMIO 0x00000000001
[ 0.000000] c0 0 (swapper) bootconsole [pxa_serial0] enabled

```

Figure 7. the master core starts normally with correctly signed kernel

At the same time, on the basis of the original, a piece of uboot code is tampered, the kernel image is generated, the image is re-burned, and the experiment board is started. The boot information can be seen from the serial port debugging tool, as shown in Figure 8. After the boot file is penetrated, the boot process verification fails and the boot is terminated.



```

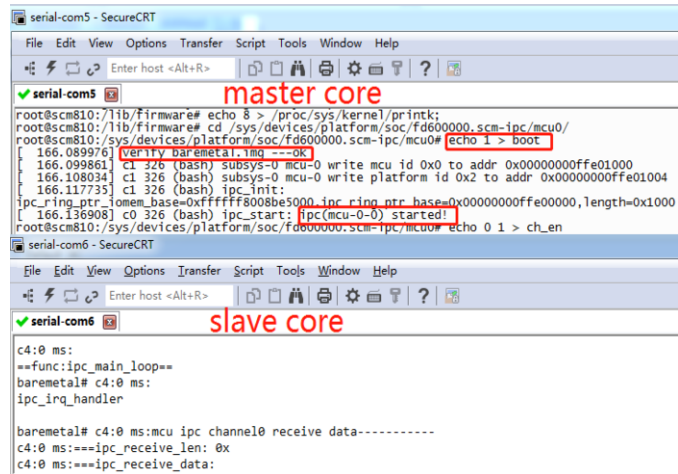
Serial-COM2104 - SecureCRT
File Edit View Options Transfer Script Tools Window Help
Enter host <Alt+R>
Serial-COM2104
Load Address: 0x82080000
Entry Point: 0x82080000
Verifying Hash Integrity ... fail
## Loading fdt from FIT Image at 87000000 ...
Using 'conf8scm810-evb.dtb' configuration
Trying 'fdt8scm810-evb.dtb' fdt subimage
Description: Flattened Device Tree Blob
Type: Flat Device Tree
Compression: uncompressed
Data Start: 0x87a9b39c
Data Size: 32448 Bytes = 31.7 KiB
Architecture: AArch64
Load Address: 0x86088000
Verifying Hash Integrity ... fail
Loading fdt from 0x87a9b39c to 0x86088000
Booting using the fdt blob at 0x86088000
compatible = "scm,scm810-evb"
scm_verify_image: image_load_addr=0x86ffffe0 image_len=0x17b75c0
scm_verify_image: verify_image:.....fail
Rebooting in 5 seconds..

BOOTROM: v4.0(release):scm_bootrom
BOOTROM: Built: 10:32:28, Jul 7 2021
sys_boot_data: 0x1c00
BOOTROM: EMMC boot
emmc_init_card, clk_src = 0x0, clk_div = 0x0
emmc: boot info version: 0x10001
BOOTROM: load sp10
BOOTROM: verify sp10
BOOTROM: skip image verify as rotphk is NULSPL: v2.1(release):scm_sp1

```

Figure 8. Validation failure of modified kernel image

To verify scenario two, as shown in Figure 9, the correctly signed baremetal.img can start normally and respond to the interrupt normally under the control of the master core linux.



```
serial-com5 - SecureCRT
File Edit View Options Transfer Script Tools Window Help
Enter host <Alt+R>

master core
root@scm810:/lib/firmware# echo 8 > /proc/sys/kernel/printk;
root@scm810:/lib/firmware# cd /sys/devices/platform/soc/fd600000.scm-ipc/mcu0/
root@scm810:/sys/devices/platform/soc/fd600000.scm-ipc/mcu0# echo 1 > boot
[ 166.089976] verify_baremetal.img ---OK
[ 166.099861] c1 326 (bash) subsys-0 mcu-0 write mcu id 0x0 to addr 0x00000000ffe01000
[ 166.108034] c1 326 (bash) subsys-0 mcu-0 write platform id 0x2 to addr 0x00000000ffe01004
[ 166.117735] c1 326 (bash) ipc_init;
ipc_ring_ptr : mem_base=0xfffff8008be5000 ipc_ring_ptr_base=0x00000000ffe00000, length=0x1000
[ 166.136908] c0 326 (bash) ipc_start: ipc(mcu-0-0) started!
root@scm810:/sys/devices/platform/soc/fd600000.scm-ipc/mcu0# echo 0 1 > ch_en

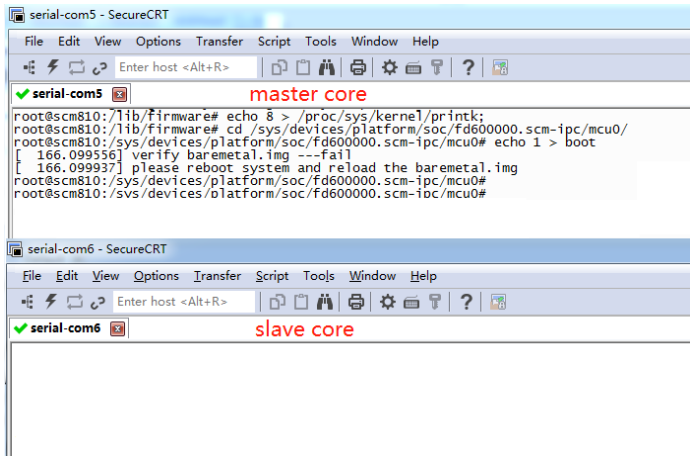
serial-com6 - SecureCRT
File Edit View Options Transfer Script Tools Window Help
Enter host <Alt+R>

slave core
c4:0 ms:
==func:ipc_main_loop==
baremetal# c4:0 ms:
ipc_irq_handler

baremetal# c4:0 ms:mcu ipc channel0 receive data-----
c4:0 ms:===ipc_receive_len: 0x
c4:0 ms:===ipc_receive_data:
```

Figure 9. the slave core starts normally with correctly signed baremetal image

At the same time, when the master core linux starts the tampered slave core code baremetal.img, the boot process fails to pass the verification and the boot is terminated. As shown in Figure 10.



```
serial-com5 - SecureCRT
File Edit View Options Transfer Script Tools Window Help
Enter host <Alt+R>

master core
root@scm810:/lib/firmware# echo 8 > /proc/sys/kernel/printk;
root@scm810:/lib/firmware# cd /sys/devices/platform/soc/fd600000.scm-ipc/mcu0/
root@scm810:/sys/devices/platform/soc/fd600000.scm-ipc/mcu0# echo 1 > boot
[ 166.099937] verify_baremetal.img ---fail
[ 166.099937] please reboot system and reload the baremetal.img
root@scm810:/sys/devices/platform/soc/fd600000.scm-ipc/mcu0#
root@scm810:/sys/devices/platform/soc/fd600000.scm-ipc/mcu0#

serial-com6 - SecureCRT
File Edit View Options Transfer Script Tools Window Help
Enter host <Alt+R>

slave core
```

Figure 10. Validation failure of modified baremetal image

5. Conclusions

In this paper, from the perspective of solving multi-core secure boot, we study a software secure boot scheme based on ARM Trustzone, which meets the security requirements of multi-core boot to a certain extent, but it needs to be further improved.

Acknowledgments

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