

CNTFET Based Fully Differential First Order All Pass Filter

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Abstract: A novel, carbon nanotube field effect transistor (CNTFET) based fully differential first order all pass filter (FDFAPF) circuit configuration is presented. The FDFAPF uses CNTFET based negative transconductors (NTs) and positive transconductors (PTs) in its realization. The proposed circuit topology employs two PTs, two NTs, two resistors and one capacitor. All the passive components of the realized topology are grounded. Active only fully differential first order all pass filter (AO-FDFAPF) topology is also derived from the proposed FDFAPF. The electronic tunability of the AO-FDFAPF is obtained by controlling the employed CNTFET based varactor. A tunability of pole frequency in the range of 10.5 to 26 GHz is obtained. Both the circuits are potential candidates for high frequency fully differential analog signal processing applications. As compared to prior state-of-the-art works, both the realized topologies have achieved highest pole frequency and lowest power dissipation. Moreover, they utilize compact circuit structures and suitable for low voltage applications. Moreover, both topologies work equally well in the deep submicron. The proposed filters are analyzed and verified through HSPICE simulations by utilizing Stanford CNTFET model at 16 nm technology node. It is observed that the proposed circuit simulation outcomes verify the theory.

Keywords: Fully differential; CNTFET; all pass filters; pole frequency; tunability

1 Introduction

Fully differential processing of analog signals is of great importance especially in case of high speed or high frequency applications [1]. As compared to single ended circuit configurations, the fully differential topologies provide better suppression to common mode as well as power supply noise, larger output dynamic range and reduced even order harmonics [2]. However, the cost for these benefits ultimately increased the circuit design complexity [3]. For modern mixed mode analog signal processing (ASP) applications, fully differential circuit configurations play a significant role. Mixed-mode signal processing applications attracts considerable attention of researchers as it simplifies the design, reduces cost and enables compactness [4]. However, interference of signal from digital-part to the analog-part remains a challenging issue to overcome; hence, for such circuit applications fully differential building blocks are recognized as a good solution since it give immunity to the digital-noise [5]. Thus, the fully differential circuits find broad range of applications in many analog modules [1–9].



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The first order all pass filter (APF) is an important multipurpose ASP module utilized for realization of higher order frequency selective circuits, quadrature and multiphase oscillators as well as phase equalizers etc [10]. Several APFs are reported in the technical literature [11–15]. However, majority of these filters lack the advantages of fully differential topologies. Moreover, these filter circuits consume considerably high power and are also not suitable for high frequency applications. Few FDFAPF topologies based on efficient active building block like negative second generation current conveyor [4], differential voltage dual-X current conveyor [16], electronically controlled current conveyors [17], digitally controlled differential voltage current conveyor [18–20], adjustable current amplifier [21], differential current conveyor [22], operational transconductance amplifier [23] and differential voltage current conveyor [24,25] etc are available in the technical literature. However, these topologies suffer with high power consumption [21,25], large number of transistor count [16,18–21,23–25] and low operating pole frequency [4,16,17,19–25]. Also, the FDFAPF circuits of [4,16,22,24,25] lack the tunability feature.

It is to be noted that FDFAPF circuits proposed in the technical literature [4,16,17,19–25] utilize bulk semiconductor technology which faces several emerging issues due to continuous focus on device scaling in nano meter scale for further validation of Moore's law. These includes short channel effects, lithographic limitations, gate leakage, boron penetrations, high field effects, poly-silicon depletion and increased heat production etc [26,27]. There is an essential requirement to substitute the conventional bulk semiconductor technology with more reliable and robust circuit technology to work equally well at nano-scale. Various devices architecture has been introduced recently, like CNTFET, FinFETs, double gate FET, strained Si FET etc [28]. Among these solutions, CNTFET is considered as a promising alternative for future extension of Moore's law due to its efficient electrostatic control, ballistic transport of charge carriers, large thermal conductivity, lesser parasitics, higher cutoff frequency, large drive current and low power dissipation to name a few [26–28]. Since introduction of CNTFET as an emerging device and better alternative of bulk semiconductor technology, limited work on CNTFET based circuit design has been carried out in analog filtering domain [10,18,26,27,29,30].

This work aims to realize new APF topologies with compact circuit structures for low voltage, low power and high frequency fully differential applications. In this paper, initially a voltage mode CNTFET based novel FDFAPF is presented. The FDFAPF has a compact circuit topology, and it uses grounded passive components only. The proposed FDFAPF employs two NTs, two PTs, two resistors and one capacitor. AO-FDFAPF is also derived from the FDFAPF, which is free from any external passive component. The proposed AO-FDFAPF offers a tunable pole frequency in the range of 10.5 to 26 GHz. In addition, both the circuit are good candidates for low voltage, low power and high frequency ASP applications. The proposed filter circuits are simulated with HSPICE using Stanford CNTFET model. The HSPICE simulation outcomes thus obtained substantiate the proposed theory. This paper is organized into six sections: Section 2 provides a brief overview of CNTFET based transconductors while Section 3 explains the proposed filter. Section 4 presents the design and verification while Section 5 discusses comparison of the proposed work with other FDFAPF. The final section presents the conclusions from this work.

2 CNTFET Based NT and PT

The NT and PT are compact ABBs with single input/output [29]. The two CNTFETs based realization of NT with its symbol and parasitic model are shown in Figs. 1a–1c respectively. The NT input port has parasitic capacitance (C_{in}) in parallel to resistance ($R_{in} = 1 / G_{in}$) while its output port has parasitic capacitance (C_{on}) in parallel to parasitic resistance ($R_{on} = 1 / G_{on}$). The four CNTFETs based realization of PT with its symbol and parasitic model are shown in Figs. 2a–2c respectively. The PT input port has parasitic capacitance (C_{ip}) in parallel to parasitic resistance ($R_{ip} = 1 / G_{ip}$) while its output port has parasitic capacitance (C_{op}) parallel

to parasitic resistance ($R_{op} = 1 / G_{op}$). The port relationships of input and output of an ideal NT and PT active elements can be defined respectively through following equations:

$$I_{no} = -V_i g_m \tag{1}$$

$$I_{po} = V_i g_m \tag{2}$$

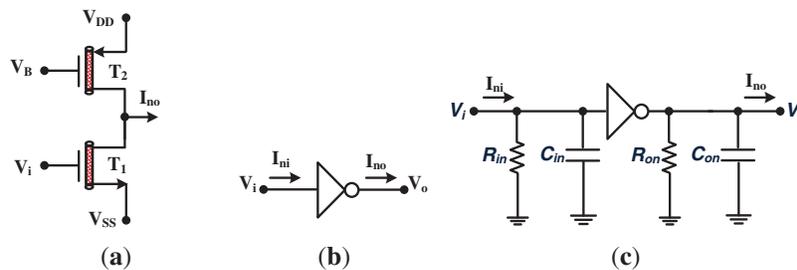


Figure 1: The NT (a) CNTFET realization (b) symbol (c) parasitic model

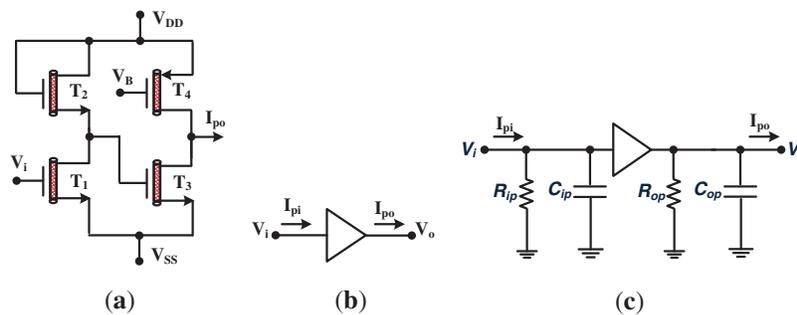


Figure 2: The PT (a) CNTFET realization (b) symbol (c) parasitic model

Here, g_m is the transconductance of the PT and NT ABBs. The CMOS based ASP circuit design is based on MOSFETs aspect ratio, while the CNTFET based circuit design is optimized with pitch (S_{CNT}), number of CNTs (N_{CNT}), and diameter (D_{CNT}) [10,29]. The width (W) of CNTFET is given as:

$$W = (S_{CNT} * (N_{CNT} - 1)) + D_{CNT} \tag{3}$$

The CNTFET D_{CNT} and threshold-voltage (V_{th}) are given as [29]:

$$D_{CNT} = \frac{a\sqrt{(m^2 + n^2 + nm)}}{\pi} \tag{4}$$

$$V_{th} = \frac{0.43}{D_{CNT}} \tag{5}$$

where, a is graphene lattice constant and (m, n) are chirality vector indices [26]. In this work, the Stanford CNTFET model is used for the circuit verification [31]. This model accurately predicts the transient and AC performance with more than 90% of accuracy and take care of numerous non idealities like effect of drain-source extension region, charge-screening-effect, inter-CNT interconnect wiring capacitance, finite scattering mean free path, drain to source series resistance and many more [10,26].

3 Proposed Filter Circuits

The proposed FDFAPF topology is shown in Fig. 3. The realized circuit utilizes NTs and PTs as an ABB. The circuit is based on two PTs, two NTs, two grounded resistors and one grounded capacitor. Ignoring the parasitics of employed NTs and PTs, and by considering $g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_m$, the routine analysis of the Fig. 3, yields the following voltage transfer-function.

$$\frac{V_{od}}{V_{id}} = g_m R_1 \left(\frac{sC + \frac{1}{R_2} - \frac{1}{R_1}}{sC + \frac{1}{R_2}} \right) \quad (6)$$

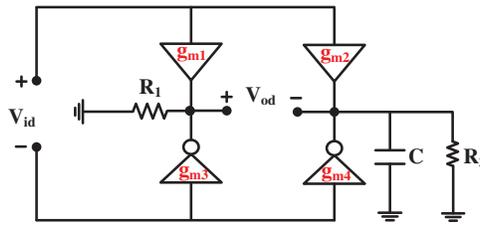


Figure 3: Proposed FDFAPF circuit

If $g_m * R_1 = 1$ and $R_2 = 2R_1$, an FDFAPF will be realized, with the voltage transfer-function:

$$\frac{V_{od}}{V_{id}} = \frac{s - \frac{1}{R_2 C}}{s + \frac{1}{R_2 C}} \quad (7)$$

From Eq. (7), the pole/zero frequency and phase angle of the FDFAPF can be written as:

$$\omega_p = \omega_z = \omega_o = \frac{1}{R_2 C} \quad (8)$$

$$\phi = \pi - 2 \tan^{-1}(\omega R_2 C) \quad (9)$$

The incremental sensitivity of the realized FDFAPF pole frequency with respect to the passive components R_2 and C can be obtained as:

$$S_{R_2}^{\omega_o} = S_C^{\omega_o} = -1 \quad (10)$$

From Eq. (10), it is evident that the sensitivity of the pole frequency of FDFAPF with respect to passive component C and R_2 are unity in magnitude.

The AO-FDFAPF topology is shown in Fig. 4. This topology is derived from Fig. 3, where resistance R_1 and R_2 are replaced by negative feedback NTs ABB and capacitance C by a CNTFET varactor. The CNTFET based varactor utilized by AO-FDFAPF is given in Fig. 5. Ignoring the parasitics of employed NTs and PTs, and by considering $g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_{m5} = g_m$ and $g_{m6} = g_m/2$, the transfer-function of the AO-FDFAPF can be determined as:

$$\frac{V_{od}}{V_{id}} = \frac{s - \frac{g_m}{2C}}{s + \frac{g_m}{2C}} \quad (11)$$

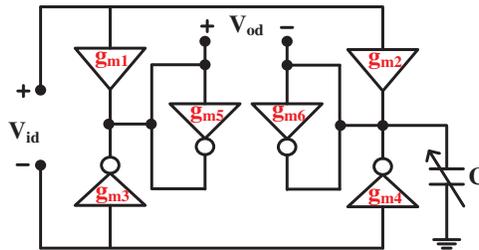


Figure 4: Proposed AO-FDFAPF circuit

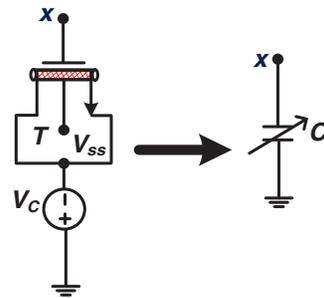


Figure 5: Realized varactor using CNTFET

From Eq. (11), the pole/zero frequency and phase angle of the AO-FDFAPF can be written as:

$$\omega_p = \omega_z = \omega_o = \frac{g_m}{2C} \quad (12)$$

$$\phi = \pi - 2 \tan^{-1} \left(\frac{2\omega C}{g_m} \right) \quad (13)$$

From Eqs. (12) and (13) it is evident that the pole/zero frequency and phase of AO-FDFAPF are dependent on varactor capacitance (C). Thus, the tunability of phase angle can be achieved through control voltage (V_C) of the varactor.

The Eq. (11) is obtained under the ideal-conditions and do not consider the influence of NT and PT ABBs input and output ports parasitics. Fig. 6 demonstrates the non ideal equivalent circuit of realized AO-FDFAPF. The overall parasitics at each individual node due to non ideal behavior of NTs and PTs are shown in Fig. 6.

The impact of these non-idealities on the proposed circuit voltage transfer-function is given by following expression.

$$\frac{V_{od}}{V_{id}} = \frac{g_m}{(g_m + G_y)} * \frac{s(C + C_z - C_y) - \frac{g_m}{2} - (G_z - G_y)}{\left(s(C + C_z) + \frac{g_m}{2} + G_z\right) * \left(1 + \frac{sC_y}{(g_m + G_y)}\right)} \quad (14)$$

where,

$$G_w = G_{ip1} + G_{ip2} \quad (15)$$

$$C_w = C_{ip1} + C_{ip2} \quad (16)$$

$$G_X = G_{in3} + G_{in4} \quad (17)$$

$$C_X = C_{in3} + C_{in4} \quad (18)$$

$$G_y = G_{op1} + G_{on3} + G_{in5} + G_{on5} \quad (19)$$

$$C_y = C_{op1} + C_{on3} + C_{in5} + C_{on5} \quad (20)$$

$$G_z = G_{op2} + G_{on4} + G_{in6} + G_{on6} \quad (21)$$

$$C_z = C_{op2} + C_{on4} + C_{in6} + C_{on6} \quad (22)$$

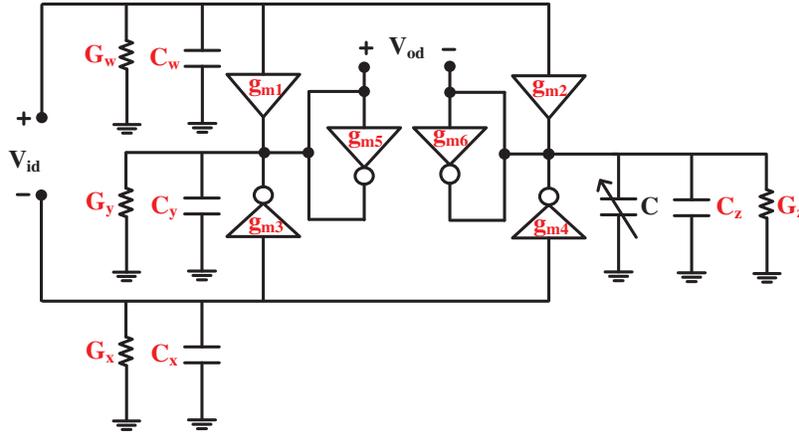


Figure 6: AO-FDFAPF with parasitics

It is evident from [29], that the parasitic capacitance associated with NT and PT ABBs are in order of aF and also parasitic conductance are in the order of nS. As $g_m \gg G_y$, $g_m \gg G_z$, $G_y \approx G_z$, $C \gg C_z$, $C_y \approx C_z$ and $C_y/(G_y + g_m) \ll 1$, the Eq. (14) reduces to Eq. (11). Thus, the impact of non-idealities on performance of the proposed AO-FDFAPF circuit are insignificant.

4 Design and Verification

To verify the behavior of proposed FDFAPF and AO-FDFAPF, the HSPICE simulations have been performed with 0.7 V supply voltage. The Stanford model with CNTFET parameters ($L_g = 16$ nm, $L_s = 16$ nm, $L_d = 16$ nm, $n = 19$, $m = 0$, $V_{fbn} = 0$, $T_{ox} = 3$ nm, $K_{ox} = 25$, $L_{eff} = 15$ nm, $L_{ceff} = 200$ nm, $K_{sub} = 4$, $S_{CNT} = 10$ nm and $E_{fo} = 0.6$ eV) has been used for verification [26]. Fig. 7 demonstrate the NT and PT frequency response of transconductance with different number of tubes (N_{CNT}). It is noticed that the PT and NT provide almost constant transconductance over 100 GHz frequency range. This constant

value of transconductance over a wide range of frequency makes the PT and NT as a good candidate for high frequency applications. It is also observed, that with increasing N_{CNTs} , the transconductance of NT and PT ABBs increases [29].

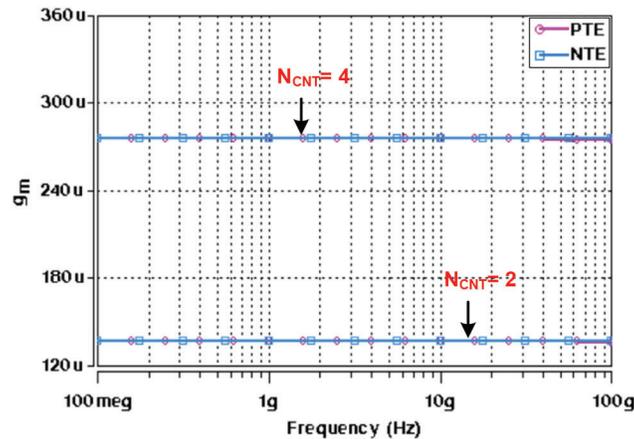


Figure 7: NT and PT transconductance (g_m) frequency response with different N_{CNTs}

The FDFAPF circuit of Fig. 3 is designed to meet the requirement of Eq. (6) to realize the all-pass response at pole frequency $f_o = 10.9$ GHz, with $N_{CNT} = 4$ for all CNTFETs of the NTs and PTs. This results $C = 2$ fF, $R_1 = 3.63$ K Ω and $R_2 = 7.26$ K Ω . The Figs. 8 and 9 demonstrate the ideal and simulated gain and phase frequency responses at a design pole frequency of 10.9 GHz, where it is observed that the simulated results, almost matched with the theoretical predictions. The observed transient behavior of the FDFAPF at designed pole frequency is given in Fig. 10, which clearly demonstrates a phase shift of 90° between differential input and output. The observed power dissipation in the designed FDFAPF is 0.66 mW. The Fig. 11 represents the input and output noise simulation results which are found as 22.461 nV/ \sqrt{Hz} and 22.257 nV/ \sqrt{Hz} respectively, at the designed frequency of 10.9 GHz, which are of insignificant magnitudes. Monte Carlo (MC) analysis of FDFAPF with 30 runs for AC and transient responses are also carried out to investigate the impact of process variations. Figs. 12 to 14 show the outcomes of the FDFAPF MC analysis for gain, phase and transient responses respectively, from which it is evident that there are no significant variations on the FDFAPF performance.

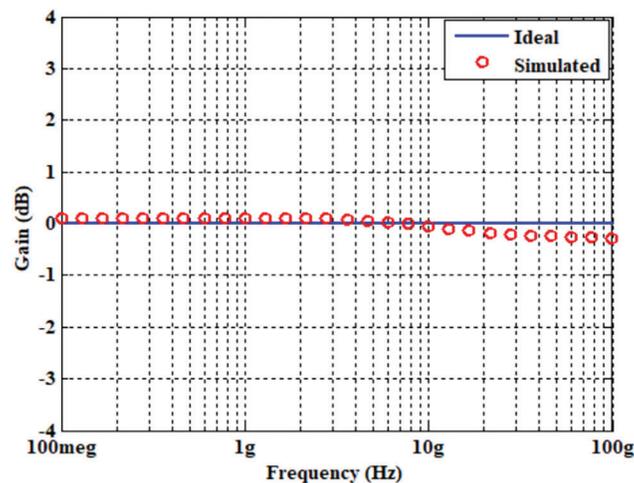


Figure 8: Ideal and simulated frequency response of voltage gain of FDFAPF

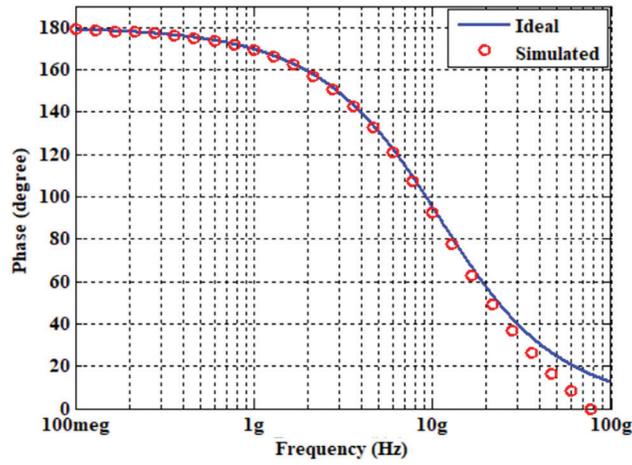


Figure 9: Ideal and simulated frequency response of phase of FDFAPF

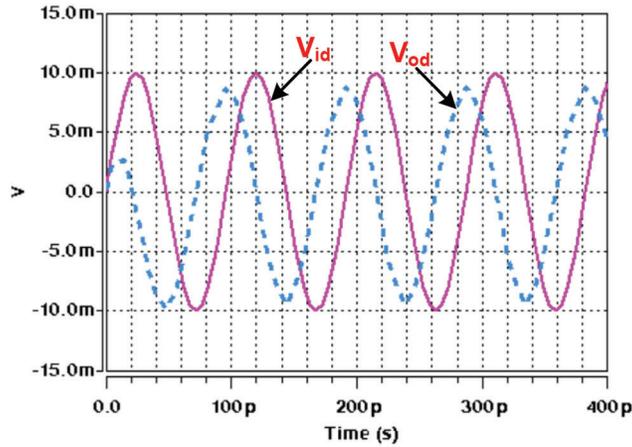


Figure 10: Transient response of FDFAPF at $f_0=10.9$ GHz

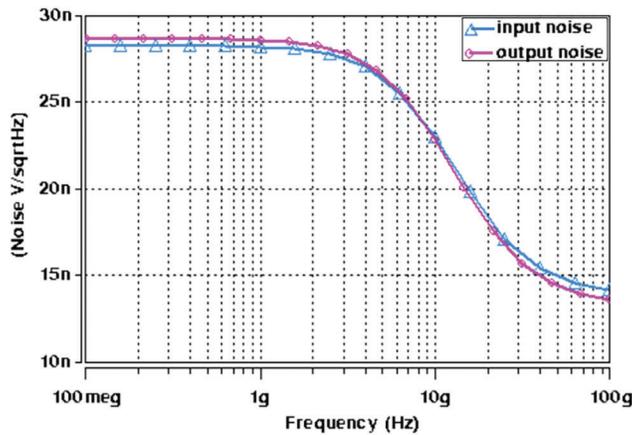


Figure 11: Frequency response of input output noise of FDFAPF

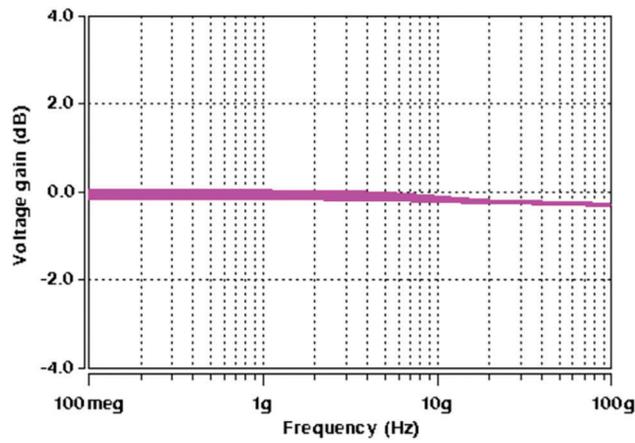


Figure 12: MC simulations of FDFAPF gain

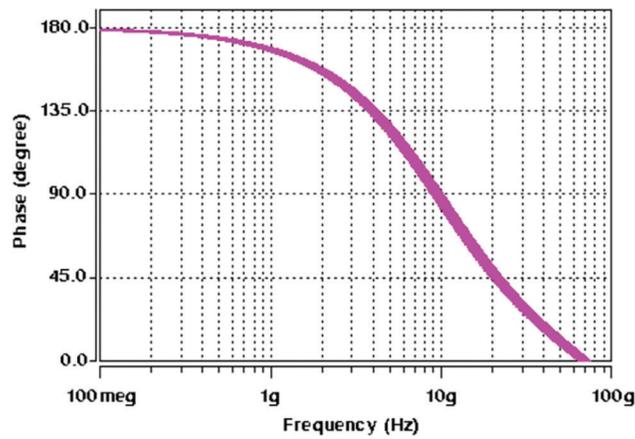


Figure 13: MC Simulations of FDFAPF phase

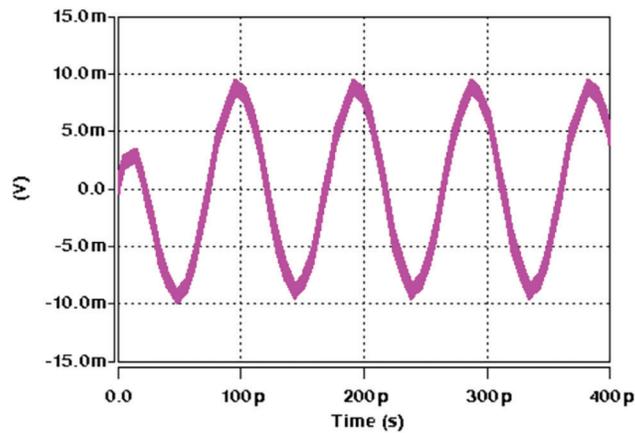


Figure 14: MC Simulations of FDFAPF transient

Fig. 15 shows the capacitance-voltage simulation results of N-Type CNTFET varactor of Fig. 5, which is utilized in the design of AO-FDFAPF. It is realized with $N_{CNT} = 229$. It is seen that by altering the varactor

tune voltage (V_C) from -0.4 V to -0.2 V, the capacitance (C) changes from 2 fF to 0.24 fF. This wide range of capacitance variation by controlling V_C , is the key to wide tunability feature of the realized AO-FDFAPF. The AO-FDFAPF circuit of Fig. 4 was also simulated with $[N_{CNT6} = 2, N_{CNTi} = 4]$, where N_{CNT6} are the number of tubes utilized for CNTFETs of transconductor 6 and N_{CNTi} are the number of tubes of CNTFETs utilized by all other transconductors to full-fill the primary requirements ($g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_{m5} = g_m$ and $g_{m6} = g_m/2$). Figs. 16 and 17 show the gain and phase frequency response results respectively for the AO-FDFAPF, at different values of control voltage (V_C). It is observed from Fig. 17, that by altering the V_C from -0.4 V to -0.25 V, the AO-FDFAPF pole frequency changes in the range of 10.5 to 26 GHz.

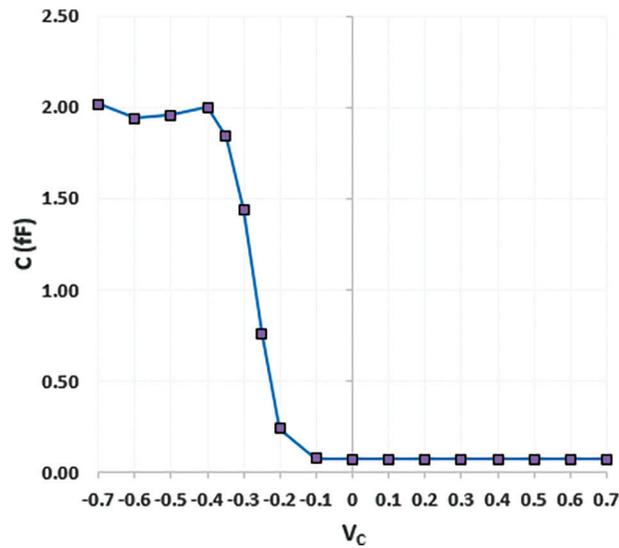


Figure 15: CV characteristics of varactor with $N_{CNT} = 229$

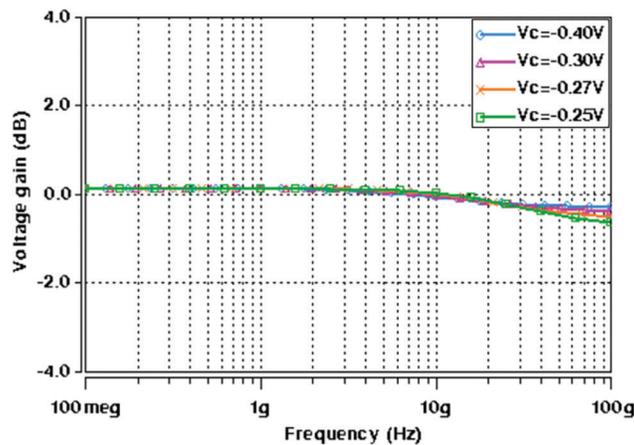


Figure 16: Frequency response of AO-FDFAPF gain at different values of V_C

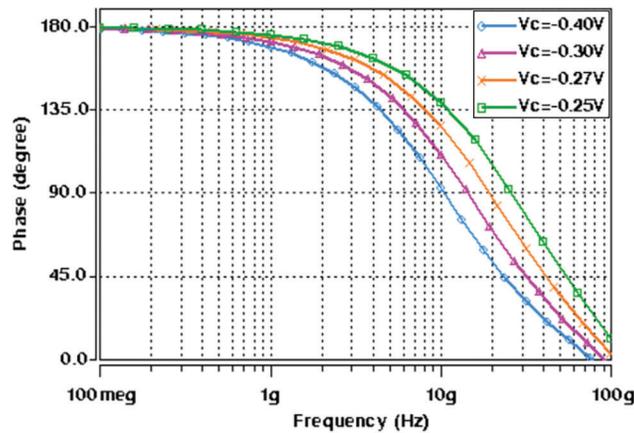


Figure 17: Frequency response of AO-FDFAPF gain at different values of V_C

5 Comparative Study

The [Tab. 1](#) demonstrates comparison of the proposed circuits with some other relevant FDFAPF reported in the open literature till date. It is seen that the FDFAPF of [Fig. 3](#) is compact and utilizes lowest active components count as compared to reported FDFAPFs [[16–21,23–26](#)]. The APF of [[22](#)] also utilizes twelve transistors, however it uses more passive components. Majority of reported APF [[16,17,19–26](#)] have frequency limitations where frequency range is limited to few MHz only. The APF of [[18](#)] works in the GHz range, however it is based on large number of active and passive components. The AO-FDFAPF of [Fig. 4](#) which is derived from proposed FDFAPF of [Fig. 3](#), does not use any external passive component and thus appropriate for integration. Both the reported filters consume less power as compared to other reported FDFAPFs. It is also to be noted that APF of [[16,22,24](#)] are not tunable, however the proposed AO-FDFAPF is tunable for wide band of frequencies.

Table 1: Comparison with reported FDFAPF topologies

Reference	No. of transistors	No. of R/C	grounded passive Components	Mode	Technology-node, Supply voltage	Tunability, range (Hz)	Power (mW)
4	18	3/1	No	Voltage	0.35 μm , ± 2.5	No, \sim	–
16	30	3/2	No	Voltage	0.25 μm , ± 1.25	No, \sim	–
17	–	5/1	No	Voltage	–	Yes, 227 K to 959 K	–
18	64	3/3	No	Voltage	32 nm, ± 0.9	Yes, 100 M to 1.5 G	–
19	92	2/2	No	Voltage	0.25 μm , ± 2.5	Yes, 31.85 K-477 K	–
20	76	4/2	No	Current	0.5 μm , ± 2.5	Yes, 1.59 M-11.1 M	–
21	54	0/1	No	Current	0.18 μm , ± 1.2	Yes, 239 K-1.41 M	5.29

(Continued)

Table 1 (continued)

Reference	No. of transistors	No. of R/C	grounded passive Components	Mode	Technology-node, Supply voltage	Tunability, range (Hz)	Power (mW)
22	12	3/1	No	Voltage	0.18 μm , ± 0.9	No, \sim	–
23	31	0/4	No	Voltage	0.5 μm , ± 0.9	Yes, 50K to 1 M	–
24	18	3/1	No	Voltage	0.5 μm , ± 2.5	No, \sim	–
25	52	1/1	No	Voltage	0.18 μm , ± 0.9	No, \sim	2.38
FDFAPF	12	2/1	Yes	Voltage	16 nm, ± 0.7	No, \sim	0.66
AO-FDFAPF	17	0/0	\sim	Voltage	16 nm, ± 0.7	Yes, 10.5 G to 26 G	0.83

Note: \sim not applicable; - not mentioned

6 Conclusion

In this paper, two novel CNTFET based voltage mode fully differential first order all pass filters are presented. Both the proposed topologies utilize CNTFET based compact negative and positive transconductors. The first topology utilizes few transistors and grounded passive components. The second topology is active only fully differential all pass filter derived from the first topology. The tunability of the active only filter is achieved through a single CNTFET based varactor. The ideal and non ideal circuit performance are investigated for the realized filter. Both the filter circuits are simulated with HSPICE by utilizing well known Stanford CNTFET model. The simulation outcomes demonstrate excellent gain, phase and transient characteristics for proposed circuits at high frequencies. The active only filter circuit, demonstrates a wide tunable pole frequency. Moreover, both the filter topologies work equally well on low voltages and dissipate considerable low power. Thus, the proposed filters are ideal candidates for low voltage, low power and high frequency fully differential applications. The simulation outcomes on the proposed filter circuits verify the theoretical predications.

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Conflicts of Interest: The authors declare that they have no conflicts of interest to report regarding the present study.

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