# An In-Band Full-Duplex Transceiver Prototype with an In-System Automated Tuning for RF Self-Interference Cancellation

Mina Mikhael<sup>1,2</sup>, Barend van Liempd<sup>2</sup>, Jan Craninckx<sup>2</sup>, Rafik Guindi<sup>1</sup>, Björn Debaillie<sup>2</sup> <sup>1</sup>Nile University, Egypt <sup>2</sup>Imec, Belgium

inice, Deigiuni

Abstract—This paper presents a transceiver prototype capable of in-band full duplex communication. Apart from a conventional transceiver and antenna, this prototype relies on a tunable electrical balance duplexer to minimize the in-band self-interference at RF. Such duplexer however requires continuous-time tuning to ensure accurate impedance balancing with the antenna across different environmental conditions. An automatic tuning algorithm is presented which tracks antenna impedance variations and tunes the duplexer accordingly. This tuning operates on a standard compliant training sequence to minimize the overhead on the communication system. The implemented tuning mechanism does not require any additional RF or analog hardware, and maximally re-uses the digital resources of a conventional baseband processor. The full duplex prototype was validated in a wireless link for IEEE802.11 channels in the 2.4GHz ISM band, in which the error vector magnitude improves by 15dB as the RF self-interference cancellation increased from 25dB to 45dB.

Keywords—In-band full duplex, self-interference cancellation, automated tuning, transceiver prototype.

## I. INTRODUCTION

Data traffic over wireless networks is rapidly increasing in the limited wireless spectrum. To provide this growing necessity, communication systems offering higher spectral efficiency are needed [1]. In-band full duplex (FD) has the potential to increase the spectral efficiency by using radios which simultaneously transmit and receive within the same frequency band. Theoretically, the spectral efficiency is doubled while using FD compared to the conventional frequency-division duplexing (FDD), which utilizes different frequency bands for transmission and reception, and the time-division duplexing (TDD), which time-interleaves transmission and reception.

The main FD challenge is located in the wireless radio, where transmitter (Tx) signals leak into its own receiver (Rx) and cause self-interference. Typically, the Tx signal is 100dB higher than the Rx noise floor [2] which leads to the degradation of the Rx signal to noise ratio (SNR). In recent literature, several RF, analog and digital self-interference cancellation (SIC) techniques have been proposed [1]. Given the tough SIC requirement, a combined design is required where the selfinterference is cancelled constructively at different locations in the radio.



Fig. 1. In-band FD transceiver with automated tuning for self interference cancellation.

Recently, the electrical balance duplexer (EBD) has been proposed as a promising RF SIC technique [2-4] which enables dense integration in compact and portable radio devices. The EBD interfaces a conventional single-port antenna with the Tx and Rx while isolating the Tx and Rx signal paths. This work uses a prototype EBD CMOS chip [2,3]. Using an EBD, the SIC is limited by the accuracy of the impedance balance between the antenna and a tunable on chip impedance, the socalled balance network. In the prototype, the balance network is constructed as a parallel network consisting of a tunable resistor (R) and a tunable capacitor (C). Both R and C are individually tunable through a digital interface.

In a realistic operating condition, wireless devices are subjected to a-priori unknown environmental scenarios, including changes in the antenna environmental conditions (e.g. device mobility, moving objects), leading to unknown antenna impedance values. To maintain a high SIC across such conditions when using an EBD for RF SIC, an automated tuning mechanism is required that accurately balances the balance network impedance with the antenna impedance.

This work proposes a transceiver (TRx) prototype as depicted in Figure 1, that avoids the need for additional analog or RF circuitry apart from the EBD to enable FD operation, and implements an in-system automated tuning algorithm in

The research leading to these results has received funding from the European Union Seventh Framework Programme under grant agreement no.316369 project DUPLO: www.fp7-duplo.eu

the digital baseband to monitor the SIC and to perform the tuning accordingly. In this paper, only this RF SIC technique is implemented. In order to satisfy the 100dB SIC requirements as discussed earlier, additional digital SIC can be used as shown in [5]. In Section II and III, the development of the tuning algorithm and how it can be efficiently integrated in the FD operation is presented. Section IV describes the prototype validation setup and illustrates FD performance measurements over a wireless communication link.

# II. AUTOMATED TUNING ALGORITHM

In an EBD, the SIC is quantified by the antenna impedance  $(Z_{ant})$  and the balance network impedance  $(Z_{bal})$  [6], as follows:

$$SIC_{Tx-Rx}(dB) \propto -20log_{10}(|\Gamma_{ant}(\omega) - \Gamma_{bal}(\omega)|)$$
 (1)

where

$$\Gamma_{ant} = \frac{Z_{ant}(\omega) - Z_o}{Z_{ant}(\omega) + Z_o}$$
(2)

and

$$\Gamma_{bal} = \frac{Z_{bal}(\omega) - Z_o}{Z_{bal}(\omega) + Z_o} \tag{3}$$

In order to achieve the maximum SIC,  $\Gamma_{bal}(\omega)$  should be balanced with  $\Gamma_{ant}(\omega)$  across the channel bandwidth i.e. have the same frequency dependency. When operating in FDD mode, sufficient SIC is required for both the Tx and Rx bands. In contrast, we only need a balance condition across a single frequency band, as the Tx and Rx operate concurrently at the same frequency. For example, to enable FDD, a complex balance network configuration would be required [7]. In our case, a simple balance network that consists of a variable R in parallel with a variable C was used. In order to achieve maximum SIC for this balance network,  $|\Delta\Gamma| = |\Gamma_{ant}(\omega) - \Gamma_{bal}(\omega)|$  should be minimized across the channel bandwidth.

Equation (1) is exploited to develop an intelligent tuning algorithm which uses the measured SIC value to quantify the balance network impedance in order to reduce  $|\Delta\Gamma|$  and improve the SIC. The usage of (1) allows the tuning algorithm to be parameterized for efficient tuning, and enables machine learning over multiple iterations.

The tuning algorithm is executed in two main phases. The first phase is the training and modeling phase. In this phase, the algorithm is trained to characterize the effect of digitally controlling the balance network on the SIC. By using data fitting techniques on the observed training points, a model of the circuit behavior is formed. This phase should be done once per chip after fabrication but should also be updated to improve the accuracy of the model across different operating conditions.

During the second phase, the tuning is performed during system operation. The model first uses the measured SIC value to estimate  $|\Delta\Gamma|$  based on (1). Then, a search algorithm identifies the actual phase of  $\Delta\Gamma$ . This second step is required as the SIC value is based on the magnitude  $|\Delta\Gamma|$  only, but lacks the phase angle information. After finding  $\Delta\Gamma$ , the model is used again to determine the required change in the R/C codes to minimize this difference. Figure 2 shows the flowchart of the tuning algorithm during operation. The medium access control



Fig. 2. The flowchart of the tuning algorithm during FD operation.



Fig. 3. An example of the training data-set for the SIC versus resistance and capacitance codes.

(MAC) layer is responsible for initiating the tuning algorithm. The main criterion to effectively re-tune after initiation from the MAC depends on a pre-defined SIC threshold which depends mainly on the application.

## A. Phase I: Training and Modelling

The training phase gathers a data-set that describes the relation between the SIC and the R/C codes during constant antenna impedance conditions. As this data-set is gathered after fabrication, it includes the chip-to-chip process variations. Moreover, in order to increase the reliability of the modelling, the data-set can be updated during the TRx lifetime. Although this measurement requires constant antenna impedance conditions, it can be executed in a realistic environment since normal

antenna impedance dynamic (tens of milliseconds [8]) are slower than the whole training phase (tens of microseconds).

Figure 3 shows an example of the data-set gained from the training phase. The data-set covers the entire range of R/C codes. A coarse set of these codes can also be used in practice to minimize the measurement time, as long as the SIC surface pattern is sufficiently captured. Based on the obtained dataset, a mathematical model is derived by fitting the theoretical equations that describe the circuit.

The least squares method was used for data fitting, by using (1-3) in combination with the theoretical relationship between the R/C codes and the estimated balance network impedance:

$$C = C_{const} + k_{c1}C_{code}(0:3) + k_{c3}C_{code}(4:7) + k_{c3}C_{code}(8:11)$$
(4)

$$R = \begin{cases} R_{const} / / \frac{k_r}{(R_{code}V_D - V_{th})^{\alpha}} & , R_{code} \ge \frac{V_{th}}{V_D} \\ R_{const} & , R_{code} < \frac{V_{th}}{V_D} \end{cases}$$
(5)

where R and C are the model values for the resistor and capacitor in the balance network impedance. Rcode and Ccode are the R/C codes of the resistance and the capacitance.  $C_{const}$ ,  $k_{c1}$ ,  $k_{c2}$ ,  $k_{c3}$ ,  $R_{const}$ ,  $V_D$ ,  $V_{th}$ ,  $\alpha$  and  $k_r$  are data fitting parameters derived from the theoretical equations describing the balance network impedance. After fitting of the training data-set to the Equations (1-5), the model will include the best-fit values of  $Z_o$  and the parameters in (4,5) to provide:

- The relation between the measured SIC and  $|\Delta\Gamma|$  (1).
- The relation between the modeled balance network impedances R and C versus the R/C codes (4,5) as shown in Figure 4.
- The relation between ΔΓ and the antenna impedance (2,3) where the balance network impedance is determined from (4,5) by using the current R/C codes.

By using this model and the measured SIC, the phase of  $\Delta\Gamma$  is the only missing variable to calculate the R/C codes that balance the EBD and minimize the SIC.

## B. Phase II: Angular Search Algorithm

During system operation, the balance network is tuned by estimating  $|\Delta\Gamma|$  from applying the measured SIC in the model derived in the previous phase. But as the antenna impedance is a complex value, the magnitude value  $|\Delta\Gamma|$  only is not sufficient for proper quantification. Therefore, an angular search algorithm is required to determine also the phase of  $\Delta\Gamma$ to be able to use the model to find the required R/C codes.

This technique relies on changing the phase of  $\Delta\Gamma$  while maintaining its magnitude (determined by the measured SIC). Using the model again, the system can determine the change in the corresponding R/C codes needed to test this specific phase as shown previously using (1-5). By applying these R/C codes and measuring the corresponding SIC, the search algorithm can find the optimum phase. As an illustration of this process, Figure 5 shows the measured SIC in function of phase-rotating the balance network impedance. Over 360° degrees phase rotation, the SIC shows a bell-shape behaviour only one maximum and one minimum. Figure 5 shows an



Fig. 4. The model of the balance network resistance and capacitance versus R and C codes.



Fig. 5. An example of the measured relation of SIC with the phase angle of  $\Delta\Gamma$  showing the two paths from the minimum SIC to the maximum SIC.

important property in the curve where any phase near the maximum SIC will always have higher SIC than further phase. This shape enables the usage of efficient search techniques to determine the optimum phase towards which the balance network impedance needs to be tuned.

The angular search starts as illustrated in Figure 6, when the system measures the SIC in its current situation (point 0) below its determined threshold. Next, the system measures three SIC measurements of which the angle of  $\Delta\Gamma$  is 120° degrees spaced as illustrated with a (point 1). Based on the SIC values in these three points, the algorithm will limit its search between the two angles with highest SIC; For example, if the highest SIC were at 120° and 240° phase angle, the search algorithm then will continue by testing the angle in middle (180° phase angle). This process then repeats until the optimum angular phase is found. Note however that the



Fig. 6. An example of the development of the angular search in terms of R and C codes.

points on Figure 6 are not ideally circular, although the  $|\Delta\Gamma|$  magnitude remains constant. That is because the relation is not linear between the digital R/C codes and the effective reflection coefficient values.

#### III. IMPLEMENTATION

The prototype setup is illustrated in Figure 7. It includes a Wireless open-Access Research radio Platform (WARP) version 3 [9], the EBD CMOS chip-prototype [3] and a commercial planar inverted-F antenna (PIFA). WARPv3 integrates a high performance FPGA (Xilinx Virtex-6) and embeds two RF-TRx interfaces. Each TRx interface can be configured to operate in Tx or Rx mode. The PC acts as the interface between WARPv3 and the EBD. The WARPlab v7.4 framework was used to perform data acquisition, while the main signal processing such as the tuning algorithm and calculating the SIC is performed on the PC.

The radio platform is configured for simultaneous Tx and Rx operation in the same channel, in which one RF interface is configured as Tx and the other as Rx. Both WARPv3 and the EBD are configured for operation in the IEEE802.11 channels in the 2.4GHz ISM band.

Note that this prototype uses commercial off-the-shelf halfduplex components. Apart from the EBD, no dedicated analog circuitry or special antenna structures are required to enable FD operation. All signal processing, including monitoring and tuning, is performed digitally and will be implemented in the FPGA. This makes the prototype commercially attractive and convenient for design and development.

Evidently, the tuning algorithm requires dedicated signal processing in digital baseband. To preserve the digital design complexity, the tuning algorithm has been developed to maximally reuse the digital hardware resources of conventional OFDM-based TRx processors. The tuning algorithm for example, samples the output of the Rx FFT, and thus reuses much of the Rx digital hardware resources and functionalities.



Fig. 7. The setup of the prototype.

RF hardware tuning is generally a burden: it obstructs normal TRx operation during tuning and it requires special training/test sequences which may be standard-incompliant. The presented tuning algorithm has been developed to overcome this burden by operating on the short training sequence (STS) which is part of every IEEE802.11 packet. The STS is used mainly by the remote radio node for packet detection and automatic gain control. In this paper, we propose to use it simultaneously in the local node for SIC performance monitoring and to activate the impedance tuning when needed. In this way, the tuning can happen while preserving normal transmitter operation with only the receiver off (half-duplex (HD) mode). Once the required SIC is achieved, the transceiver can then restore its full FD capability.

In the IEEE802.11 standard, each STS consists of ten identical short symbols (800ns each). Each short symbol has the same frequency pattern which consists of 12 sub-carriers distributed over the channel bandwidth. The characteristics of the STS are also useful for the SIC tuning algorithm as:

- Using specific frequency pattern allows enhanced detection in noisy ethers by using e.g. cross-correlation processing or averaging over consequent frequency responses.
- Using short symbols (800ns) allows for faster tuning compared to the longer training sequences.
- Using multiple identical symbols allows multiple tuning steps over the consequent symbols.

The only modification that will be required in the current standard to utilize the STS in the tuning algorithm, is increasing the number of symbols in the STS to satisfy the tuning algorithm requirements. Note that this overhead in the STS will be required only in the one packet at the tuning phase. For each tuning step, one symbol can be used to measure the SIC. After each measurement, processing is needed to calculate the next step which needs another one or more symbols according to the digital processing capability.

## IV. RESULTS

The FD transceiver prototype, including the automated tuning algorithm of the EBD solution, has been tested in several realistic operation conditions. The automated tuning was tested by using the standard compatible STS. Our solution provides an average SIC across the 20MHz wide channel up to 50dB. Note that using smaller bandwidth signals for validation would improve the total SIC due to the narrow-band behavior of the EBD (originally designed for smaller bandwidths [3]), but is no longer representative for IEEE802.11.

Different environmental scenarios were tested (e.g. antenna movement, placing nearby metal objects, hand movement, etc.). These different scenarios impact the antenna impedance and cause imbalance with the impedance of the (un-tuned) balance network which will degrade the SIC as illustrated in Figure 8 at tuning step (0). After starting, the tuning algorithm steps towards an improved SIC for each different scenario; Figure 8 indicates that the required SIC values are achieved after about 10 tuning steps. Given this low amount of tuning steps, efficient and rapid re-tuning with minimum overhead on the communication operation is enabled.

Another set of measurements are performed based on a wireless communication link between two radio nodes. The local radio node (the prototype described in this paper) is operating in FD, i.e. simultaneously transmitting and receiving on the same frequency band, where the remote node is transmitting the data of interest. The local node demodulates the received signal of interest and extracts the constellation diagram.

Recent literature [2,8] shows that FD wireless link requires more than 100dB SIC in order operate with the standard specifications (typical range, data rate, etc.). In order to achieve this SIC requirements, multiple SIC solutions should be combined. Additional digital SIC technique may be implemented in the baseband section (future work) to achieve the required specifications. Using only one SIC solution (<50dB) results in a limited link distance and transmission power of the local FD node. In our setup, the transmit power of the remote node was set to 10dBm, and the transmit power of the local link was varied (0dBm, -10dBm, -20dBm) over short wireless link distance ( $\sim$ 15 cm).

Figure 9 shows the measured constellation diagram before activation of the tuning algorithm (SIC of 20dB) and after (SIC of 50dB). The tuning algorithm clearly improves the reception performance of the wireless link towards an error vector magnitude (EVM) of -30dB. Figure 10 shows the measured EVM versus the achieved SIC level. The balance network impedance was controlled to achieve the varying SIC values and the EVM of the FD link was measured at each value. The figure shows the direct relation between the SIC and the EVM of the link.

In the IEEE802.11 standard, the duration of each symbol in the STS is 800ns. From our results, the required number of tuning steps can be in range of ten steps, which implies a time overhead for the tuning in the range of tens of micro-seconds as shown in Section III. Since the antenna impedance variation is much slower; typically in the range of tens of milli-seconds [8], our results demonstrate the practical feasibility of EBD tuning for in band FD operation.



Fig. 8. The SIC during the tuning algorithm operation in different environmental variations.



Fig. 9. The constellation diagrams of the FD link at (a) SIC = 50 dB (b) SIC = 20 dB (local node Tx power = -10dBm).



Fig. 10. The effect of the SIC on the EVM of the FD link with only the RF SIC solution (Assuming additional 50dB of digital SIC will compensate for transmitter power difference and the short link distance).

#### V. CONCLUSION

In-band full duplex radios design is challenged to achieve SIC values of more than 100dB. This can only be achieved with a constructive cancellation at digital, analog and RF. This work presents a development and validation prototype that utilizes an RF SIC solution based on a tunable electrical balance duplexer. To automatically tune this duplexer within the system, an algorithm was developed to achieve >45dB of RF SIC over different antenna environmental conditions and variations. The tuning mechanism has been developed for minimal footprint in terms of implementation and operation. The tuning algorithm, which is implemented in the digital baseband, does not require additional analog/RF circuitry, and it utilizes the standard compliant STS during operation in SIC monitoring and tuning for minimal overhead. Apart from the duplexer, the prototype builds on traditional radio hardware components and enables future incorporation of additional cancellation techniques (e.g. digital).

The prototype is validated over different environmental variations, and the measurements indicate efficient tuning from worst-case SIC degradations observed towards >45dB of SIC in about 10 tuning steps. Furthermore, wireless communication link between two radio nodes is tested, where the local node is operating in FD. EVM improvements of 15dB are measured as the SIC improves from 25dB to 45dB. All the measurements consider IEEE802.11 channels in the 2.4GHz ISM band.

# ACKNOWLEDGMENT

The authors would like to thank Benjamin Hershberg for the beneficial discussions and Peter Van Wesemael for his help in the FPGA implementation of the algorithm (future work).

#### REFERENCES

- A. Sabharwal, P. Schniter, D. Guo, D. W. Bliss, S. Rangarajan, and R. Wichman, "In-band full-duplex wireless: Challenges and opportunities," *IEEE J. on Sel. Areas in Commun. (JSAC)*, vol. 32, no. 9, pp. 1637–1652, Sep. 2014.
- [2] B. Debaillie, D.-J. van den Broek, C. Lavin, B. van Liempd, E. A. M. Klumperink, C. Palacios, J. Craninckx, B. Nauta, and A. Parssinen, "Analog/RF solutions enabling compact full-duplex radios," *IEEE J. on Sel. Areas in Commun. (JSAC)*, vol. 32, no. 9, pp. 1662–1673, Sep. 2014.
- [3] B. van Liempd, B. Debaillie, J. Craninckx, C. Lavin, C. Palacios, S. Malotaux, J. Long, D. van den Broek, and E. Klumperink, "Rf selfinterference cancellation for full-duplex," in 9th Int. Conf. on Cognitive Radio Oriented Wireless Networks and Commun. (CROWNCOM), Jun. 2014, pp. 526–531.
- [4] L. Laughlin, M. A. Beach, K. A. Morris, and J. L. Haine, "Optimum single antenna full duplex using hybrid junctions," *IEEE J. on Sel. Areas* in Commun. (JSAC), vol. 32, no. 9, pp. 1653–1661, Sep. 2014.
- [5] D. Korpi, L. Anttila, V. Syrjala, and M. Valkama, "Widely linear digital self-interference cancellation in direct-conversion full-duplex transceiver," *IEEE J. on Sel. Areas in Commun. (JSAC)*, vol. 32, no. 9, pp. 1674–1687, Sep. 2014.
- [6] S. H. Abdelhalem, P. S. Gudem, and L. E. Larson, "Hybrid transformerbased tunable differential duplexer in a 90-nm CMOS process," *IEEE Trans. on Microw. Theory and Tech.*, vol. 61, no. 3, pp. 1316–1326, Mar. 2013.
- [7] B. van Liempd, R. Singh, S. Malotaux, P. Reynaert, J. Long, and J. Craninckx, "A dual-notch +27dbm tx-power electrical-balance duplexer," in *European Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2014.
- [8] D. Bharadia, E. McMilin, and S. Katti, "Full duplex radios," in *Proc. of the ACM SIGCOMM 2013 Conf. on SIGCOMM*, Aug. 2013, pp. 375–386.
- [9] "Warp project," http://warpproject.org.