Panel: The World Is Going… Analog & Mixed-Signal! What about EDA?

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Panelists: Mario Anton, Micronas, Germany; Ori Galzur, TowerJazz, Israel;
Robert Hum, Mentor Graphics, USA; Rainer Kress, Infineon Technologies, Germany; Paul Lo, Synopsys, USA

Abstract

Contrarily to a common belief, the world is not going digital! Analog and mixed-signal electronics is more and more important and yet pervasive. This is due both to the increasing systems integration, by nature leading to heterogeneity, and to the complex, digital computing functions being complemented by scores of on-chip analog functions, interfacing/interacting with people, environment, and other systems. Specialty silicon foundries are now stable members of top ten revenue rankings.

This technology trend demands for more design automation in both implementation and verification domains. Lossless interfaces between digital and analog design environments, multi-technology support, mixed-signal simulation engines – but also debugging aids – are no longer a nice to have. According to IBS [1], the cost of implementing and verifying the mixed-signal functions is generally over 50% of the design costs even though the mixed-signal transistors can be as low as 3% of the total!

What are the critical requirement, moving forward, and what is EDA industry doing to serve the needs of this increasingly important semiconductor industry segment?

Moderator's Introduction

Pietro Palella, STMicroelectronics, Italy

The first observation is that what is surrounding humans substantially behaves in an "analog" manner.

The need to interact more and more with people and the environment is driving the increasing importance of the "More than Moore" trend, heavily dominated by analog and mixed signal designs to interface with sensors, actuators and MEMs.

In the last decade the EDA industry has been primarily focused on the evolution of the digital design tools, improving their features and performance to follow the "More Moore" trend, characterized by deep submicron technologies and very complex digital designs.

In the meantime, significant portions of the analog and mixed signal designs have often been "handcrafted" by experienced designers, with a little level of automation, without the attention of the EDA industry they would have deserved.

The fast evolution of the silicon technologies allows the integration of several large functions in very dense and small dice with not only electrical but also other physical behaviors, such as mechanic.

This capability permits to design complete systems in single dice and their complexity requires a much higher level of design automation and verification capabilities crossing the barriers of physical domains.

Extending the concept of systems and considering they have to be more and more "eco-sustainable" in terms of, for instance, power consumption and noise emission, the capability to co-design and verify chips, packages and boards becomes a must.

It is evident and obvious that today the designers have to face significant challenges that can only become more difficult.

EDA has to play the role and take the challenge to help and facilitate the life of the analog and mixed signal design experts.

Most of the analog and mixed signal design steps have room for improvements in terms of user interface, features, performance and overall automation.

A closer cooperation between the EDA industry and the design community could significantly improve the current scenario. Let's move on and … good luck!

Panelists' Position Statements

Mario Anton, Micronas, Germany

Representative for the overall industry trend, in the domain of HALL based sensor systems for automotive applications Micronas sees strongly increasing requirements resulting in more advanced analog circuitry and growing digital content. Basic drivers for this trend are amongst others:

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• Smart and robust systems, higher sensor resolution

• More flexible circuit interfaces (analog, digital) and communication protocols, more compute power

• Increasing safety requirements such as diagnosis functions and redundancy

Increasing complexity and the continuous demand for development cycle time reduction drive the challenges for design and verification methodologies. A combined top-down/bottom up design methodology (on analog side mainly driven by analog feasibility issues and/or area limitations), tailored to product specific characteristics is the key to success. Verification strategies that allow co-simulation of analog and digital circuitry on several abstraction levels (from concept to chip-level signoff simulation) need to be applied. Different circuit representations to accomplish this are available: analog, discrete real-type, digital, behavioral modeling – in the meantime supported by a variety of design tools. It is strongly recommended to tailor the different verification approaches with respect to circuit complexity and functionality (Micronas examples: from simple analog sensor to Analog and Mixed-Signal (AMS) SoC with embedded controller). Apart from the availability of EDA tools it is important to consider that such approaches add further complexity to project execution, to name a few examples:

• Required skills (e.g. behavioral modeling, AMS verification experts,…) need to be built up in the project teams, respective responsibilities to be assigned

• Common sense to be found on number and purpose of AMS simulations being done during different design stages (proof of concept, toplevel interface checks and/or functional toplevel simulations,…)

• Project planning needs to consider required AMS specific work steps and task dependencies (review and updates of behavioral models, complex verification plans, interaction design & layout,…)

Without proper consideration of these aspects, AMS projects will not execute best in class.

EDA vendors have released numerous tools and methods to support AMS designs. Nonetheless we still face challenges that need to be addressed to close the gap between the time to market requirements and the growing complexity of AMS designs. EDA industry needs to provide further solutions, to be aligned with their customer base - some examples:

• Increase AMS simulation speed while keeping accuracy, consequent device model (HV, RF, LP) support for the complete tool chain

• AMS reference flows (or reference use cases) that can be tailored

• Tool flexibility (e.g. coupling of different simulation engines, design hierarchy, A/D interfaces, waveform viewing and debugging capabilities,…)

• Test bench re-use during the verification of different abstractions levels (system, digital, discrete real type, AMS & analog) – up to lab evaluation and test?!

• AMS verification planning methods, AMS and analog coverage

Beyond traditional design and verification topics new challenges arise especially for the execution of Automotive AMS products. We expect EDA vendors to address new areas like:

• Verification planning methods that provide interfaces to requirements management tools, e.g. allowing parameter and requirement traceability

• Tools that allow assessment of fault metrics and diagnosys coverage (as requested by ISO26262), faults injection in analog design,…

• Simulation of aging effects, ESD simulation, aids for the automation for high voltage stress tests (e.g. how are overvoltages propagated into analog circuitry?)

Ori Galzur, TowerJazz, Israel

As the design and fabrication world in steaming down the critical dimensions to achieve performance and cost, addressing the challenges of a wireless and green world, the analog part of the system becomes very difficult catching up and staying cost effective.

Especially with deep submicron designs that have naturally low voltages and high frequencies, the interface IC's to the analog world become key to the success. These IC's still need to address several parameters that do not scale down, such as high voltages, high rate ESD and many customizations.

The analog IC's generally share similar requests:

1) Fast time to market, fast design cycle.

2) Low cost, small die size.

3) Low cost of design (EDA tools, FAB process steps, first time success rate)

Foundries that support such design must have answers to the above. This requires a modular PDK, support variance of EDA flows and very fast turnaround from masking to manufacturing process.

This opens many new opportunities for foundry/EDA collaborations to supply a full solution kit that will be friendly, cost effective on one hand while on the other hand give designers the benefits of the powerful tools available today.

Many of the interfaces IC's do not require design nodes beyond 130 nanometers; however the challenge of a small die with respect to high ESD and high voltage tolerance is quite difficult. The PDK's must include new feature sets to address the above, and the ability to simulate DFM is a major differentiator for those who provide these features. Some examples, having an ERC checker that will flag ESD violations and HV violations can save few design cycles and prevent bugs previously detected only in the lab when its already too late. These and other examples open an opportunity for EDA to innovate in the older technologies and increase their market share in a world that many though had past. The solution that will be a strongly supported by foundries will give renaissance to the design tools and design methodologies that were stagnant for many years.

Analog designs will become more and more critical and can easily make the difference of a winning system. Those who will be clever enough to merge the new tools and features with the old school analog design flow will come out winners. EDA innovation in the analog world is critical piece of the puzzle and we have just begun.

Robert Hum, Mentor Graphics, USA

Strictly speaking, our universe is very digital with modern quantum theories pointing not only to the quantization of energy, but also to that of time and space. In a broad sense this is actually good news for EDA: quantization, or more correctly, discretization, is what enables EDA to deal with what appear to be continuous domain phenomena. We very aptly use discretization in space (grids, meshes, tessellations) as well as in time (SPICE for example) to solve what would otherwise require closed form or analytic solutions. The question "What about EDA?" is meant to address the lack of progress in advancing the state of the art in productivity as well as perhaps the lack of broad cohesive functionality for increasingly critical, complex and advanced analog and mixed-signal circuits at small geometries (taking into account electro-thermal effects, electromagnetic effects, mechanical stress, electrical stress, etc. in a single tool flow). It is instructive to recall the underpinnings of progress in the digital domain, where today's leading edge designs would have overwhelmed the design tools available, say, 5 years ago. EDA has made amazing advances in tools that drive productivity forward in the digital domain. It has only accomplished this with the very close and willing cooperation of the design community however. Progress in the digital domain has been made through the use of abstraction and encapsulation! At one time logic was designed at the transistor level, then at the gate level, then at the RTL level, and now even at the behavioral level. Each jump in abstraction brought with it a new design methodology that was adopted broadly by the design community and optimized through supporting tools by the EDA community. In a very large and important way, it was really the broad adoption of a 'standard design methodology' (hierarchical cooperating finite state machines for example) that enabled EDA to make progress with tools such as synthesis, static timing verification, digital verification, library characterization, design rule checking, emulation, place and route and so forth.

The EDA community has been working diligently on tools to improve many aspects of analog and mixed-signal design, but let's face it; progress hasn't been as spectacular as with digital circuits. Why not? EDA greatly benefits from broadly adopted methodologies: they are a great target for optimization and automation. The analog world is, well, broad: RF design is a very different from, say, Op Amp design or filter design. Designers in these domains approach their jobs from different points of view and hence want to use different tools. I believe that progress in the EDA analog and mixed-signal world is, as we learned with digital circuits, highly dependent on the broad adoption of 'standard design methodologies'. We are, as a joint design and EDA community, making progress with analog and mixed-signal tools. With closer cooperation, the development of a few standard design methodologies (easier said than done) and some compromises (on both sides) I believe that we can do much better.

Rainer Kress, Infineon Technologies, Germany

The business of Infineon focuses on three key markets: energy efficiency, mobility, and security. Energy management is a common theme across all our target markets. The power semiconductors within the energy efficiency market are high-power devices where current density is the most critical design parameter. The mobility market has the challenge to reduce fuel consumption and CO2 emissions. We are helping the automobile OEMs to meet the new standards for CO2 emissions with our low-power solutions. The security market, especially the chip card sector has strongest requirements towards low power. When a contact less chip card draws its power from a card reader it needs to have sophisticated low-power techniques to address active and standby leakage currents.

Many of the designs at Infineon are analog and mixed-signal (AMS) designs with significant parts of analog and smaller parts of digital content. This brings challenges such as seamless analog / digital integration, verification efficiency including the AMS verification performance, reuse of AMS designs, cost of test for AMS structures, reliability and lifetime safety.

Part of Infineon's strategy is an even stronger understanding of our customers' systems. This means a

move to more comprehensive multi-domain system modeling techniques. This will serve three major purposes: fast simulation of our products in the customer application, product architecture exploration, and a seamless link to the implementation design flow. This is especially true for the analog-mixed signal part.

Historically, the EDA industry has invested significantly in enabling productive and high-quality digital designs using advanced process technologies. Results are good and have supported Moore's law for many years. Now, EDA has to follow the increasing trend towards "More than Moore" design starts. EDA should focus towards AMS to deliver automation solutions that we have on the digital design today. AMS system-level design must become a driving force for EDA incorporating thermal and mechanical effects, package issues, electromagnetic interference, etc. The system-level needs a seamless interface towards implementation of low-power AMS designs. The next level of AMS system verification on all levels needs to be investigated to cope with the increasing complexity. We need industry standard interfaces to exchange easily between tools on different abstraction levels, as well as between different EDA suppliers. Moreover, the various analog and digital models on different abstraction level have to be verified against each other. Legacy requirements have to be taken into account since "More than More" technologies tend to have a much higher lifetime than advanced technology nodes.

Paul Lo, Synopsys, USA

For over 50 years, integrated circuit (IC) manufacturing processes have been geared to supporting increasingly complex *digital* electronic systems on silicon. Each new manufacturing process focused on delivering higher performance, lower power consumption, smaller area, and cheaper *digital* gates. The common belief was that everything could be made *digital*, and that analog would eventually disappear. However, there is a growing trend where the systems integration roadmap is driving the need for more analog functionality to interface with the real world. Conversely, analog demands for more digital functionality to process real world data it senses, and to react appropriately. It does not matter if the resulting system is digital with embedded analog or viceversa: both are required, and analog will not disappear in the foreseeable future.

Digital designers use faster, cheaper gates to integrate high-performance processors, which, in turn, demand faster interface circuits with high levels of analog processing. Processor I/O subsystems are now a major mixed-signal focus for many analog IP design teams. Due to shrinking market windows and scarce analog design resources, silicon-proven, reusable mixed-signal IP is now required, not only earlier in their design cycle, but at emerging manufacturing processes, such as 20 and 16/14 nanometers. As a result, analog and mixed-signal (A&M/S) methodologies, tools, and flows are aligning with digital, and EDA does provide increasingly seamless integration of digital and A&M/S design and verification capabilities to boost productivity. For example, communication between IC place-and-route and custom layout tools is now a reality. Today, automatic custom routers integrated within digital place-and-route systems enable higher layout productivity to quickly produce complex parallel I/O busses with resistance matching; SERDES twisted pairs; shielded buses for memories and so on. In turn, place-and-route tools are able to close digital blocks in an analog IC within the allotted real estate and the tight routing resources.

Design managers indicate that digital engineering skills are less scarce than analog design talent and, with digital gates so cheap and plentiful, many designers use digital gates to trade off some analog functions – often referred to as digitally-assisted analog. For example, as designs move to emerging manufacturing processes it becomes more practical and effective to shift analog signal processing and tuning to digital circuits, such as embedded processors. However, while these techniques simplify the analog part of the design, they complicate verification with the need for fast, yet highly accurate, mixed-signal verification. EDA is extending powerful testbench and automated checking capabilities typically used in the digital verification world to address the needs of mixed-signal SoC designs. For certain design applications, such as automotive electronics, there is a reliability requirement to thoroughly validate functionality of the system with multiple design environment constraints and exhaustive testing. As such, the drive for fast mixed-signal verification to support regression testing is a must have going forward and will likely drive a new round of innovation within the EDA community over the next several years.

Many systems applications require more than just plain CMOS devices: BCD applications include the power management that is so critical to make batteries last longer, as well as to increase their lifespan; RF applications include the ubiquitous global positioning system (GPS), Bluetooth, and Wi-Fi; CMOS image sensor applications include rear-view automotive cameras, and require large amounts of memory, and sophisticated digital processing; MEMS applications include motion sensors and microphones found in every smartphone and game console, and require a great deal of digital processing. As the integration of non-digital, micro- and nano-mechanical systems that do not scale according to Moore's Law moves from the board to the IC, it poses new challenges that EDA is addressing. As an example, multi-technology, and multi-physics device modeling and simulation plays an increasingly fundamental role.

Synopsys is fully conscious of the importance that A&M/S has reached for our partners and customers. Synopsys commitment and expertise in the A&M/S design domain goes far beyond typical software tool research and development. Today, Synopsys employs over 1,000 A&M/S designers developing mixed-signal IP products, including interconnect IP, such as USB, PCI Express®, and DDR, targeting a broad range of silicon manufacturing processes. They engage with leading foundries to implement IP using emerging manufacturing processes; taping out test chips; testing and characterizing the resulting silicon; and delivering robust, silicon-proven IP to thousands of design teams globally. They use our complete A&M/S design implementation and verification solution – the same capabilities we deliver to our customers.