

Lecture Notes in Computer Science

Edited by G. Goos, J. Hartmanis and J. van Leeuwen

1940

Springer

Berlin

Heidelberg

New York

Barcelona

Hong Kong

London

Milan

Paris

Singapore

Tokyo

Mateo Valero Kazuki Joe
Masaru Kitsuregawa Hidehiko Tanaka (Eds.)

High Performance Computing

Third International Symposium, ISHPC 2000
Tokyo, Japan, October 16-18, 2000
Proceedings



Springer

Series Editors

Gerhard Goos, Karlsruhe University, Germany
Juris Hartmanis, Cornell University, NY, USA
Jan van Leeuwen, Utrecht University, The Netherlands

Volume Editors

Mateo Valero
Universidad Politecnica de Catalunya
Departamento de Arquitectura de Computadores, Spain
E-mail: mateo@ac.upc.es

Kazuki Joe
Nara Women's University
Department of Information and Computer Sciences, Japan
E-mail: joe@ics.nara-wu.ac.jp

Masaru Kitsuregawa
University of Tokyo
Institute of Industrial Science
Center for Conceptual Information Processing Research, Japan
E-mail: kitsure@tkl.iis.u-tokyo.ac.jp

Hidehiko Tanaka
University of Tokyo
Graduate School of Engineering
Electrical Engineering Department, Japan
E-mail: tanaka@mtl.t.u-tokyo.ac.jp

Cataloging-in-Publication Data applied for

Die Deutsche Bibliothek - CIP-Einheitsaufnahme

High performance computing : third international symposium ;
proceedings / ISHPC 2000, Tokyo, Japan, October 16 - 18, 2000. Mateo
Valero ... (ed.). - Berlin ; Heidelberg ; New York ; Barcelona ; Hong
Kong ; London ; Milan ; Paris ; Singapore ; Tokyo : Springer, 2000
(Lecture notes in computer science ; Vol. 1940)
ISBN 3-540-41128-3

CR Subject Classification (1998): D.1-2, F.2, E.4, G.1-4, J.1-2, J.3, J.6, I.6

ISSN 0302-9743

ISBN 3-540-41128-3 Springer-Verlag Berlin Heidelberg New York

This work is subject to copyright. All rights are reserved, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, re-use of illustrations, recitation, broadcasting, reproduction on microfilms or in any other way, and storage in data banks. Duplication of this publication or parts thereof is permitted only under the provisions of the German Copyright Law of September 9, 1965, in its current version, and permission for use must always be obtained from Springer-Verlag. Violations are liable for prosecution under the German Copyright Law.

Springer-Verlag Berlin Heidelberg New York
a member of BertelsmannSpringer Science+Business Media GmbH
© Springer-Verlag Berlin Heidelberg 2000
Printed in Germany

Typesetting: Camera-ready by author, data conversion by DA-Tex Gerd Blumenstein
Printed on acid-free paper SPIN: 10781323 06/3142 5 4 3 2 1 0

Preface

I wish to welcome all of you to the International Symposium on High Performance Computing 2000 (ISHPC 2000) in the megalopolis of Tokyo. After having two great successes with ISHPC'97 (Fukuoka, November 1997) and ISHPC'99 (Kyoto, May 1999), many people have requested that the symposium would be held in the capital of Japan and we have agreed.

I am very pleased to serve as Conference Chair at a time when high performance computing (HPC) has a significant influence on computer science and technology. In particular, HPC has had and will continue to have a significant impact on the advanced technologies of the "IT" revolution. The many conferences and symposiums that are held on the subject around the world are an indication of the importance of this area and the interest of the research community.

One of the goals of this symposium is to provide a forum for the discussion of all aspects of HPC (from system architecture to real applications) in a more informal and personal fashion. Today we are delighted to have this symposium, which includes excellent invited talks, tutorials and workshops, as well as high quality technical papers.

In recent years, the goals, purpose and methodology of HPC have changed drastically. HPC with high-cost, high-power consumption and difficult-to-use interfaces will no longer attract users. We should instead use what the IT revolution of the present and near future gives us: highly integrated processors and extremely fast internet. Mobile and wearable computing is already commonplace and the combination with multimedia and various database applications is promising. Therefore we would like to treat HPC technologies as systems and applications for low-end users as well as conventional high-end users, where we can find a bigger market. In this symposium, we will discuss the direction of such HPC technologies with hardware, software and applications specialists.

This symposium would not have been possible without the significant help of many people who devoted resources and time. I thank all of those who have worked diligently to make the ISHPC 2000 a great success. In particular I would like to thank the Organizing Chair, Masaru Kitsuregawa of the University of Tokyo, and all members of the organizing committee, who contributed very significantly to the planning and organization of ISHPC 2000. I must also thank the Program Chair, Mateo Valero of the Technical University of Catalunya, and the program committee members who assembled an excellent program comprising a very interesting collection of contributed papers from many countries.

A last note of thanks goes to the Kao Foundation for Arts and Science, the Inoue Foundation for Science, the Telecommunications Advancement Foundation and Sumisho Electronics Co. Ltd for sponsoring the symposium.

Foreword

The 3rd International Symposium on High Performance Computing (ISHPC 2000 held in Tokyo, Japan, 16–18 October 2000) was thoughtfully planned, organized, and supported by the ISHPC Organizing Committee and collaborative organizations.

The ISHPC 2000 Program consists of two keynote speeches, several invited talks, two workshops on OpenMP and Simulation-Visualization, a tutorial on OpenMP, and several technical sessions covering theoretical and applied research topics on high performance computing which are representative of the current research activities in industry and academia. Participants and contributors to this symposium represent a cross section of the research community and major laboratories in this area, including the European Center for Parallelism of Barcelona of the Polytechnical University of Catalunya (UPC), the Center for Supercomputing Research and Development of the University of Illinois at Urbana-Champaign (UIUC), the Maui High Performance Computing Center, the Kansai Research Establishment of Japan Atomic Energy Research Institute, Japan Society for Simulation Technology, SIGARCH and SIGHPC of Information Processing Society Japan, and the Society for Massively Parallel Processing.

All of us on the program committee wish to thank the authors who submitted papers to ISHPC 2000. We received 53 technical contributions from 17 countries. Each paper received at least three peer reviews and, based on the evaluation process, the program committee selected fifteen regular (12-page) papers. Since several additional papers received favorable reviews, the program committee recommended a poster session comprised of short papers. Sixteen contributions were selected as short (8-page) papers for presentation in the poster session and inclusion in the proceedings.

The program committee also recommended two awards for regular papers: a distinguished paper award and a best student paper award. The distinguished paper award was given to “Processor Mechanisms for Software Shared Memory” by Nicholas Carter, and the best student paper award was given to “Limits of Task-Based Parallelism in Irregular Applications” by Barbara Kreaseck.

ISHPC 2000 has collaborated closely with two workshops: the International Workshop on OpenMP: Experiences and Implementations (WOMPEI) organized by Eduard Ayguade of the Technical University of Catalunya, and the International Workshop on Simulation and Visualization (IWSV) organized by Katsunobu Nishihara of Osaka University. Invitation-based submission was adopted by both workshops. The ISHPC 2000 program committee decided to include all papers of WOMPEI and IWSV in the proceedings of ISHPC 2000.

We hope that the final program will be of significant interest to the participants and will serve as a launching pad for interaction and debate on technical issues among the attendees.

October 2000

Mateo Valero

Foreword from WOMPEI

First of all, we would like to thank the ISHPC Organizing Committee for giving us the opportunity to organize WOMPEI as part of the symposium. The workshop consists of one invited talk and eight contributed papers (four from Japan, two from the United States and two from Europe). They report some of the current research and development activities related to tools and compilers for OpenMP, as well as experiences in the use of the language. The workshop includes a panel discussion (shared with ISHPC) on Programming Models for New Architectures. We would also like to thank the Program Committee and the OpenMP ARB for their support in this initiative. Finally, thanks go to the Real World Computing Partnership for the financial support to WOMPEI. We hope that the program will be of interest to the OpenMP community and will serve as a forum for discussion on technical and practical issues related to the current specification.

E. Ayguade (Technical University of Catalunya),
H. Kasahara (Waseda University) and
M. Sato (Real World Computing Partnership)

Foreword from IWSV

Recent rapid and incredible improvement of HPC technologies has encouraged numerical computation users to use larger and therefore more practical simulations. The problem such high-end users face is how to analyze or even understand the results calculated with huge computation times. The promising solution to this problem is the use of visualization.

IWSV is organized as part of ISHPC 2000 and consists of 11 contributed papers and abstracts. We would like to thank the ISHPC 2000 Organizing Committee for providing us with this opportunity. We would also like to thank the ISHPC 2000 Program Committee for having IWSV papers and abstracts included in the proceedings, which we did not expect.

We hope that IWSV will be of fruitful interest to ISHPC 2000 participants and will indicate a future direction of collaboration between numerical computation and visualization researchers.

K. Nishihara (Osaka University),
K. Koyamada (Iwate Prefectural University) and
Y. Ueshima (Japan Atomic Energy Research Institute)

Organization

ISHPC 2000 is organized by the ISHPC Organizing Committee in cooperation with the European Center for Parallelism of Barcelona of the Polytechnical University of Catalunya (UPC), the Center for Supercomputing Research and Development of the University of Illinois at Urbana-Champaign (UIUC), the Maui High Performance Computing Center, the Kansai Research Establishment of Japan Atomic Energy Research Institute, Japan Society for Simulation Technology, SIGARCH and SIGHPC of Information Processing Society Japan, and the Society for Massively Parallel Processing.

Executive Committee

General Chair:	Hidehiko Tanaka (U. Tokyo, Japan)
Program Chair:	Mateo Valero (UPC, Spain)
Program Co-chair:	Jim Smith (U. Wisconsin, US)
	Constantine Polychronopoulos (UIUC, US)
	Hironori Kasahara (Waseda U., Japan)
Organizing Chair:	Masaru Kitsuregawa (U. Tokyo, Japan)
Publication & Treasuary Chair:	Kazuki Joe (NWU, Japan)
Treasuary Co-chair:	Toshinori Sato (KIT, Japan)
Local Arrangement Chair:	Hironori Nakajo (TUAT, Japan)
Poster Session Chair:	Hironori Nakajo (TUAT, Japan)
Workshop Chair:	Eduard Ayguade (UPC, Spain)
	Katsunobu Nishihara (Osaka U., Japan)

Organizing Committee

Eduard Ayguade (UPC)	Hiroki Honda (UEC)
Yasuhiro Inagami (Hitatch)	Kazuki Joe (NWU)
Yasunori Kimura (Fujitsu)	Tomohiro Kudoh (RWCP)
Steve Lumetta (UIUC)	Hironori Nakajo (TUAT)
Mitaro Namiki (TUAT)	Toshinori Sato (KIT)
Yoshiki Seo (NEC)	Chau-Wen Tseng (UMD)
Ou Yamamoto (TEU)	

Program Committee

Yutaka Akiyama (RWCP)	Mitsunori Miki (Doshisha U.)
Hideharu Amano (Keio U.)	Prasant Mohapatra (MSU)
Hamid Arabnia (Geogea U.)	Jose Moreira (IBM)
Utpal Banerjee (Intel)	Shin-ichiro Mori (Kyoto U.)
Taisuke Boku (U. Tsukuba)	Hironori Nakajo (TUAT)
George Cybenko (Dartmouth)	Takashi Nakamura (NAL)
Michel Dubois (USC)	Hiroshi Nakasima (TUT)
Rudolf Eigenmann (Purdue U)	Alex Nicolau (UCI)
Joel Emer (Compaq)	Michael L. Norman (UIUC)
Skevos Evripidou (U. Cyprus)	Theodore Papatheodorou (U. Patras)
Ophir Frieder (IIT)	John Rice (Purdue U.)
Mario Furnari (CNR)	Eric Rotenberg (NCSU)
Stratis Gallopoulos (U. Patras)	Yousef Saad (UMN)
Dennis Gannon (U. Indiana)	Mitsuhisa Sato (RWCP)
Guang Gao (U. Delaware)	Yoshiki Seo (NEC)
Antonio Gonzalez (UPC)	Guri Sohi (U. Wisconsin)
Thomas Gross (ETHZ/CMU)	Peter R. Taylor (SDSC)
Mohammad Haghighat (Intel)	Chau-Wen Tseng (UMD)
Hiroki Honda (UEC)	Dean Tullsen (UCSD)
Elias Houstis (Purdue U.)	Sriram Vajapeyam (IIS)
Yasuhiro Inagami (Hitachi)	Alex Veidenbaum (UCI)
Kazuki Joe (NWU)	Harvey J. Wassermann (LosAlamos)
Yasunori Kimura (Fujitsu)	Harry Wijshoff (Leiden U.)
Yoshitoshi Kunieda (Wakayama U.)	Tao Yang (UCSB)
Jesus Labarta (UPC, Spain)	Mitsuo Yokokawa (JAERI)
Monica Lam (Stanford)	Hans Zima (U. Vienna)
Hans Luethi (ETHZ)	
Allen Malony (U. Oregon)	
Hideo Matsuda (Osaka U.)	

Referees

T. Araki	E. Laure	M. Satoh
L. D. Cerio	J. Lu	K. Shen
A. Chowdhury	A.D. Malony	S. Tambat
L. Chu	P. Marcuello	W. Tang
J. Duato	W. Martins	H. Tang
T. Erlebach	E. Mehofer	T. Tarui
A. Funahashi	O.G. Monakhov	J. Torres
P. Grun	E.A. Monakhova	C.-W. Tseng
T. Hanawa	S. Mukherjee	T. Uehara
T. Kamachi	E. Nunohiro	
M. Kawaba	P. Ranganathan	

Table of Contents

I. Invited Papers

Instruction Level Distributed Processing: Adapting to Future Technology	1
<i>J. E. Smith</i>	
Macroserver: An Object-Based Programming and Execution Model for Processor-in-Memory Arrays	7
<i>Hans P. Zima and Thomas L. Sterling</i>	
The New DRAM Interfaces: SDRAM, RDRAM and Variants	26
<i>Brian Davis, Bruce Jacob and Trevor Mudge</i>	
Blue Gene	32
<i>Henry S. Warren, Jr.</i>	
Earth Simulator Project in Japan — Seeking a Guide Line for the Symbiosis between the Earth and Human Beings – Visualizing an Aspect of the Future of the Earth by a Supercomputer –	33
<i>Keiji Tani</i>	

II. Compilers, Architectures and Evaluation

Limits of Task-Based Parallelism in Irregular Applications	43
<i>Barbara Kreaseck, Dean Tullsen and Brad Calder</i>	
The Case for Speculative Multithreading on SMT Processors	59
<i>Haitham Akkary and Sébastien Hily</i>	
Loop Termination Prediction	73
<i>Timothy Sherwood and Brad Calder</i>	
Compiler-Directed Cache Assist Adaptivity	88
<i>Xiaomei Ji, Dan Nicolaescu, Alexander Veidenbaum, Alexandru Nicolau and Rajesh Gupta</i>	
Skewed Data Partition and Alignment Techniques for Compiling Programs on Distributed Memory Multicomputers	105
<i>Tzung-Shi Chen and Chih-Yung Chang</i>	
Processor Mechanisms for Software Shared Memory	120
<i>Nicholas P. Carter, William J. Dally, Whay S. Lee, Stephen W. Keckler and Andrew Chang</i>	
An Evaluation of Page Aggregation Technique on Different DSM Systems	134
<i>Mario Donato Marino and Geraldo Lino de Campos</i>	

Nanothreads vs. Fibers for the Support
of Fine Grain Parallelism on Windows NT/2000 Platforms146
*Vasileios K. Barekas, Panagiotis E. Hadjidoukas,
Eleftherios D. Polychronopoulos and Theodore S. Papatheodorou*

III. Algorithms, Models and Applications

Partitioned Parallel Radix Sort 160
Shin-Jae Lee, Minsoo Jeon, Andrew Sohn and Dongseung Kim

Transonic Wing Shape Optimization Based on Evolutionary Algorithms ...172
Shigeru Obayashi, Akira Oyama and Takashi Nakamura

A Common CFD Platform UPACS 182
Hiroyuki Yamazaki, Shunji Enomoto and Kazuomi Yamamoto

On Performance Modeling for HPF Applications with ASL191
*Thomas Fahringer, Michael Gerndt, Graham Riley and
Jesper Larsson Träff*

A “Generalized k-Tree-Based Model to Sub-system Allocation”
for Partitionable Multi-dimensional Mesh-Connected Architectures 205
Jeeraporn Srisawat and Nikitas A. Alexandridis

An Analytic Model for Communication Latency in Wormhole-Switched
k-Ary n-Cube Interconnection Networks with Digit-Reversal Traffic 218
H. Sarbazi-Azad, L. M. Mackenzie and M. Ould-Khaoua

Performance Sensitivity of Routing Algorithms to Failures
in Networks of Workstations 230
Xavier Molero, Federico Silla, Vicente Santonja and José Duato

IV. Short Papers

Decentralized Load Balancing in Multi-node Broadcast Schemes
for Hypercubes 243
Satoshi Fujita and Yuji Kashima

Design and Implementation of an Efficient Thread Partitioning
Algorithm 252
*José Nelson Amaral, Guang Gao, Erturk Dogan Kocalar,
Patrick O’Neill and Xinan Tang*

A Flexible Routing Scheme for Networks of Workstations 260
José Carlos Sancho, Antonio Robles and José Duato

Java Bytecode Optimization with Advanced Instruction
Folding Mechanism 268
Austin Kim and Morris Chang

Performance Evaluation of a Java Based Chat System	276
<i>Fabian Breg, Mike Lew and Harry A. G. Wijshoff</i>	
Multi-node Broadcasting in All-Ported 3-D Wormhole-Routed Torus Using Aggregation-then-Distribution Strategy	284
<i>Yuh-Shyan Chen, Che-Yi Chen and Yu-Chee Tseng</i>	
On the Influence of the Selection Function on the Performance of Networks of Workstations	292
<i>J. C. Martínez, F. Silla, P. López and J. Duato</i>	
Combining In-Transit Buffers with Optimized Routing Schemes to Boost the Performance of Networks with Source Routing	300
<i>Jose Flich, Pedro López, Manuel. P. Malumbres, José Duato and Tom Rokicki</i>	
A Comparison of Locality-Based and Recency-Based Replacement Policies	310
<i>Hans Vandierendonck and Koen De Bosschere</i>	
The Filter Data Cache: A Tour Management Comparison with Related Split Data Cache Schemes Sensitive to Data Localities	319
<i>Julio Sahuquillo, Ana Pont and Veljko Milutinovic</i>	
Global Magneto-Hydrodynamic Simulations of Differentially Rotating Accretion Disk by Astrophysical Rotational Plasma Simulator ...	328
<i>Mami Machida, Ryoji Matsumoto, Shigeki Miyaji, Kenji E. Nakamura and Hideaki Tonooka</i>	
Exploring Multi-level Parallelism in Cellular Automata Networks	336
<i>Claudia Roberta Calidonna, Claudia Di Napoli, Maurizio Giordano and Mario Mango Furnari</i>	
Orgel: An Parallel Programming Language with Declarative Communication Streams	344
<i>Kazuhiko Ohno, Shigehiro Yamamoto, Takanori Okano and Hiroshi Nakashima</i>	
BS λ_p : Functional BSP Programs on Enumerated Vectors	355
<i>Frédéric Loulergue</i>	
Ability of Classes of Dataflow Schemata with Timing Dependency	364
<i>Yasuo Matsubara and Hiroyuki Miyagawa</i>	
A New Model of Parallel Distributed Genetic Algorithms for Cluster Systems: Dual Individual DGAs	374
<i>Tomoyuki Hiroyasu, Mitsunori Miki, Masahiro Hamasaki and Yusuke Tanimura</i>	

V. International Workshop on OpenMP: Experiences and Implementations (WOMPEI)

An Introduction to OpenMP 2.0	384
<i>Timothy G. Mattson</i>	
Implementation and Evaluation of OpenMP for Hitachi SR8000	391
<i>Yasunori Nishitani, Kiyoshi Negishi, Hiroshi Ohta and Eiji Nunohiro</i>	
Performance Evaluation of the Omni OpenMP Compiler	403
<i>Kazuhiro Kusano, Shigehisa Satoh and Mitsuhsa Sato</i>	
Leveraging Transparent Data Distribution in OpenMP via User-Level Dynamic Page Migration	415
<i>Dimitrios S. Nikolopoulos, Theodore S. Papatheodorou, Constantine D. Polychronopoulos, Jesús Labarta and Eduard Ayguadé</i>	
Formalizing OpenMP Performance Properties with ASL	428
<i>Thomas Fahringer, Michael Gerndt, Graham Riley and Jesper Larsson Träff</i>	
Automatic Generation of OpenMP Directives and Its Application to Computational Fluid Dynamics Codes	440
<i>Haoqiang Jin, Michael Frumkin and Jerry Yan</i>	
Coarse-Grain Task Parallel Processing Using the OpenMP Backend of the OSCAR Multigrain Parallelizing Compiler	457
<i>Kazuhsa Ishizaka, Motoki Obata and Hironori Kasahara</i>	
Impact of OpenMP Optimizations for the MGCG Method	471
<i>Osamu Tatebe, Mitsuhsa Sato and Satoshi Sekiguchi</i>	
Quantifying Differences between OpenMP and MPI Using a Large-Scale Application Suite	482
<i>Brian Armstrong, Seon Wook Kim and Rudolf Eigenmann</i>	

VI. International Workshop on Simulation and Visualization (IWSV)

Large Scale Parallel Direct Numerical Simulation of a Separating Turbulent Boundary Layer Flow over a Flat Plate Using NAL Numerical Wind Tunnel	494
<i>Naoki Hirose, Yuichi Matsuo, Takashi Nakamura, Martin Skote and Dan Henningson</i>	
Characterization of Disorderd Networks in Vitreous SiO ₂ and Its Rigidity by Molecular-Dynamics Simulations on Parallel Computers ...	501
<i>Hajime Kimizuka, Hideo Kaburaki, Futoshi Shimizu and Yoshiaki Kogure</i>	
Direct Numerical Simulation of Coherent Structure in Turbulent Open-Channel Flows with Heat Transfer	502
<i>Yoshinobu Yamamoto, Tomoaki Kunugi and Akimi Serizawa</i>	

High Reynolds Number Computation for Turbulent Heat Transfer in a Pipe Flow	514
<i>Shin-ichi Satake, Tomoaki Kunugi and Ryutaro Himeno</i>	
Large-Scale Simulation System and Advanced Photon Research	524
<i>Yutaka Ueshima and Yasuaki Kishimoto</i>	
Parallelization, Vectorization and Visualization of Large Scale Plasma Particle Simulations and Its Application to Studies of Intense Laser Interactions	535
<i>Katsunobu Nishihara, Hirokazu Amitani, Yuko Fukuda, Tetsuya Honda, Y. Kawata, Yuko Ohashi, Hitoshi Sakagami and Yoshitaka Suzuki</i>	
Fast LIC Image Generation Based on Significance Map	537
<i>Li Chen, Issei Fujishiro and Qunsheng Peng</i>	
Fast Isosurface Generation Using the Cell-Edge Centered Propagation Algorithm	547
<i>Takayuki Itoh, Yasushi Yamaguchi and Koji Koyamada</i>	
Fast Ray-Casting for Irregular Volumes	557
<i>Koji Koyamada</i>	
A Study on the Effect of Air on the Dynamic Motion of a MEMS Device and Its Shape Optimization	573
<i>Hidetoshi Kotera, Taku Hirasawa, Sasatoshi Senga and Susumu Shima</i>	
A Distributed Rendering System “On Demand Rendering System”	585
<i>Hideo Miyachi, Toshihiko Kobayashi, Yasuhiro Takeda, Hiroshi Hoshino and Xiuyi Jin</i>	
Author Index	593