Lecture Notes in Computer Science 1940
Edited by G. Goos, J. Hartmanis and J. van Leeuwen

Springer
Berlin
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High Performance Computing

Third International Symposium, ISHPC 2000
Tokyo, Japan, October 16-18, 2000
Proceedings

Springer

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Cataloging-in-Publication Data applied for

Die Deutsche Bibliothek - CIP-Einheitsaufnahme

High performance computing : third international symposium ;
proceedings / ISHPC 2000, Tokyo, Japan, October 16 - 18, 2000. Mateo
Valero ... (ed.). - Berlin ; Heidelberg ; New York ; Barcelona ; Hong
Kong ; London ; Milan ; Paris ; Singapore ; Tokyo : Springer, 2000
(Lecture notes in computer science ; Vol. 1940)
ISBN 3-540-41128-3

CR Subject Classification (1998): D.1-2, F.2, E.4, G.1-4, J.1-2, J.3, J.6, I.6

ISSN 0302-9743
ISBN 3-540-41128-3 Springer-Verlag Berlin Heidelberg New York

Springer-Verlag Berlin Heidelberg New York
a member of BertelsmannSpringer Science+Business Media GmbH

Printed in Germany

Typesetting: Camera-ready by author, data conversion by DA-TeX Gerd Blumenstein
Printed on acid-free paper SPIN: 10781323 06/3142 5 4 3 2 1 0

Preface

I wish to welcome all of you to the International Symposium on High Performance Computing 2000 (ISHPC 2000) in the megalopolis of Tokyo. After having two great successes with ISHPC'97 (Fukuoka, November 1997) and ISHPC'99 (Kyoto, May 1999), many people have requested that the symposium would be held in the capital of Japan and we have agreed.

I am very pleased to serve as Conference Chair at a time when high performance computing (HPC) has a significant influence on computer science and technology. In particular, HPC has had and will continue to have a significant impact on the advanced technologies of the "IT" revolution. The many conferences and symposiums that are held on the subject around the world are an indication of the importance of this area and the interest of the research community.

One of the goals of this symposium is to provide a forum for the discussion of all aspects of HPC (from system architecture to real applications) in a more informal and personal fashion. Today we are delighted to have this symposium, which includes excellent invited talks, tutorials and workshops, as well as high quality technical papers.

In recent years, the goals, purpose and methodology of HPC have changed drastically. HPC with high-cost, high-power consumption and difficult-to-use interfaces will no longer attract users. We should instead use what the IT revolution of the present and near future gives us: highly integrated processors and extremely fast internet. Mobile and wearable computing is already commonplace and the combination with multimedia and various database applications is promising. Therefore we would like to treat HPC technologies as systems and applications for low-end users as well as conventional high-end users, where we can find a bigger market. In this symposium, we will discuss the direction of such HPC technologies with hardware, software and applications specialists.

This symposium would not have been possible without the significant help of many people who devoted resources and time. I thank all of those who have worked diligently to make the ISHPC 2000 a great success. In particular I would like to thank the Organizing Chair, Masaru Kitsuregawa of the University of Tokyo, and all members of the organizing committee, who contributed very significantly to the planning and organization of ISHPC 2000. I must also thank the Program Chair, Mateo Valero of the Technical University of Catalunya, and the program committee members who assembled an excellent program comprising a very interesting collection of contributed papers from many countries.

A last note of thanks goes to the Kao Foundation for Arts and Science, the Inoue Foundation for Science, the Telecommunications Advancement Foundation and Sumisho Electronics Co. Ltd for sponsoring the symposium.

October 2000 Hidehiko Tanaka

Foreword

The 3rd International Symposium on High Performance Computing (ISHPC 2000 held in Tokyo, Japan, 16–18 October 2000) was thoughtfully planned, organized, and supported by the ISHPC Organizing Committee and collaborative organizations.

The ISHPC 2000 Program consists of two keynote speeches, several invited talks, two workshops on OpenMP and Simulation-Visualization, a tutorial on OpenMP, and several technical sessions covering theoretical and applied research topics on high performance computing which are representative of the current research activities in industry and academia. Participants and contributors to this symposium represent a cross section of the research community and major laboratories in this area, including the European Center for Parallelism of Barcelona of the Polytechnical University of Catalunya (UPC), the Center for Supercomputing Research and Development of the University of Illinois at Urbana-Champaign (UIUC), the Maui High Performance Computing Center, the Kansai Research Establishment of Japan Atomic Energy Research Institute, Japan Society for Simulation Technology, SIGARCH and SIGHPC of Information Processing Society Japan, and the Society for Massively Parallel Processing.

All of us on the program committee wish to thank the authors who submitted papers to ISHPC 2000. We received 53 technical contributions from 17 countries. Each paper received at least three peer reviews and, based on the evaluation process, the program committee selected fifteen regular (12-page) papers. Since several additional papers received favorable reviews, the program committee recommended a poster session comprised of short papers. Sixteen contributions were selected as short (8-page) papers for presentation in the poster session and inclusion in the proceedings.

The program committee also recommended two awards for regular papers: a distinguished paper award and a best student paper award. The distinguished paper award was given to "Processor Mechanisms for Software Shared Memory" by Nicholas Carter, and the best student paper award was given to "Limits of Task-Based Parallelism in Irregular Applications" by Barbara Kreaseck.

ISHPC 2000 has collaborated closely with two workshops: the International Workshop on OpenMP: Experiences and Implementations (WOMPEI) organized by Eduard Ayguade of the Technical University of Catalunya, and the International Workshop on Simulation and Visualization (IWSV) organized by Katsunobu Nishihara of Osaka University. Invitation-based submission was adopted by both workshops. The ISHPC 2000 program committee decided to include all papers of WOMPEI and IWSV in the proceedings of ISHPC 2000.

We hope that the final program will be of significant interest to the participants and will serve as a launching pad for interaction and debate on technical issues among the attendees.

October 2000 Mateo Valero

Foreword from WOMPEI

First of all, we would like to thank the ISHPC Organizing Committee for giving us the opportunity to organize WOMPEI as part of the symposium. The workshop consists of one invited talk and eight contributed papers (four from Japan, two from the United States and two from Europe). They report some of the current research and development activities related to tools and compilers for OpenMP, as well as experiences in the use of the language. The workshop includes a panel discussion (shared with ISHPC) on Programming Models for New Architectures. We would also like to thank the Program Committee and the OpenMP ARB for their support in this initiative. Finally, thanks go to the Real World Computing Partnership for the financial support to WOMPEI. We hope that the program will be of interest to the OpenMP community and will serve as a forum for discussion on technical and practical issues related to the current specification.

E. Ayguade (Technical University of Catalunya),
H. Kasahara (Waseda University) and
M. Sato (Real World Computing Partnership)

Foreword from IWSV

Recent rapid and incredible improvement of HPC technologies has encouraged numerical computation users to use larger and therefore more practical simulations. The problem such high-end users face is how to analyze or even understand the results calculated with huge computation times. The promising solution to this problem is the use of visualization.

IWSV is organized as part of ISHPC 2000 and consists of 11 contributed papers and abstracts. We would like to thank the ISHPC 2000 Organizing Committee for providing us with this opportunity. We would also like to thank the ISHPC 2000 Program Committee for having IWSV papers and abstracts included in the proceedings, which we did not expect.

We hope that IWSV will be of fruitful interest to ISHPC 2000 participants and will indicate a future direction of collaboration between numerical computation and visualization researchers.

K. Nishihara (Osaka University),
K. Koyamada (Iwate Prefectural University) and
Y. Ueshima (Japan Atomic Energy Research Institute)

Organization

ISHPC 2000 is organized by the ISHPC Organizing Committee in cooperation with the European Center for Parallelism of Barcelona of the Polytechnical University of Catalunya (UPC), the Center for Supercomputing Research and Development of the University of Illinois at Urbana-Champaign (UIUC), the Maui High Performance Computing Center, the Kansai Research Establishment of Japan Atomic Energy Research Institute, Japan Society for Simulation Technology, SIGARCH and SIGHPC of Information Processing Society Japan, and the Society for Massively Parallel Processing.

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