Topic 15+20
Multimedia and Embedded Systems

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Topic Chairpersons

This combined topic embraces two broad themes: *multimedia* and *embedded systems*. Multimedia has become an important technological innovation and plays an important role in our daily activities. It is defined as the combination of the following forms of information: text, graphics, video, and audio – referred to as multimedia formats. Traditionally, the multimedia formats were being represented in an analog form, but nowadays we are observing a migration from the analog representation to the digital representation. The digital representation of the multimedia formats proved to have certain advantages, for example easier editability and improved error resilience. However, the digital representation presented the scientific community and the industry with a sizeable problem which is the enormous size of the digital representation/information and extreme computational requirements.

The second theme covered relates to embedded systems. A technology turning point that made embedded systems an everyday reality has to be the advent of microprocessors. The technological developments that allowed single chip processors (microprocessors) made the embedded systems inexpensive and flexible. Consequently, microprocessor based embedded systems have been introduced into many new application areas. Currently, embedded programmable microprocessors in one form or another, from 8-bit micro-controllers to 32-bit digital signal processors and 64-bit RISC processors, are everywhere, in consumer electronic devices, home appliances, automobiles, network equipment, industrial control systems, etc.

Some of the driving forces behind the fast expansion of the embedded systems market relates to the proliferation of computing technologies to traditionally non-computing domains, e.g., medical instrumentation, automotive industry, the fast advances in VLSI technologies, and the tendency to replace analog signal processing with digital signal processing.

From the papers submitted to both the original topics, six papers were accepted for presentation.

The first paper, by F. Seinstra, D. Koelma, and J.-M. Geusebroek, describes a software architecture that allows image processing researchers to develop parallel applications in a transparent manner. The architecture's main component is an extensive library of low level image processing operations that can be run on distributed memory MIMD-style parallel hardware.

In the second paper, by U. Assarsson and P. Stenström, a comparative performance evaluation of a number of load distribution strategies is conducted. It is shown that several strategies suffer from a too high an orchestration overhead to provide any meaningful speedup. However, it is also indicated that by apply-

ing some straightforward tricks to get rid of most of the locking needed, it is possible to achieve interesting speedups.

The third paper, by R. Kutil, deals with a fast and efficient coding algorithm using the wavelet transform. It investigates a new algorithm with a simple and spacially oriented coefficient scan order which is suitable for parallelization.

The fourth paper, by D. Tcheressiz, B. Juurlink, S. Vassiliadis and H. Wijshoff, presents performance evaluations for the Complex Streamed Instruction architecture on a set of important image processing kernels. The Complex Streamed Instruction (CSI) set is an architectural paradigm designed to accelerate multimedia applications. These applications are characterized by streaming operations on small-width data elements such as 8-bit pixels or 16-bit audio samples. CSI instructions operate on two-dimensional data streams in a SIMD fashion and are able to process streams of arbitrary length. When evaluating the performance of the CSI architecture on a set of important image processing kernels simulation results indicate that CSI provides a speedup by a factor of up to 3.98 (2.60 on average) when compared to Sun's media ISA extension VIS. Moreover CSI scales much better than VIS with increasing bandwidth.

The fifth paper, by A. El-Mahdy and I. Watson, presents a novel vector instruction set that combines the benefits of sub-word parallelism and traditional vector processing. The proposed hardware support is meant for multimedia processing on a general purpose processor and comprises a vector based instruction set with a submatrix addressing mode that utilizes subword vectors. The authors propose also a cache prefetch optimization that exploit the two dimensional access pattern of multimedia MPEG2 video applications. Detailed simulation results suggesting that the optimized cache removes 75% of the misses are also presented.

The final paper, authored by V. Kianzad and S. S. Bhattacharyya, addresses the embedded system design issue by proposing novel partitioning and scheduling techniques that aggressively streamline interprocessor communication. The paper evaluates the benefit of using Genetic Algorithms for automatic clustering of parallel embedded applications. The two key trends in the synthesis of implementations for embedded processors are addressed: the increasing importance of managing interprocessor communication in an efficient manner and the acceptance of significantly longer compilation time by embedded system designers.

In closing, we would like to thank the authors who submitted a contribution, as well as the Euro-Par Organizing Committee, and the scores of referees, whose efforts have made this conference, and the Multimedia and Embedded Systems topics possible.