

Lecture Notes in Computer Science
Edited by G. Goos, J. Hartmanis, and J. van Leeuwen

2451

Springer

Berlin

Heidelberg

New York

Barcelona

Hong Kong

London

Milan

Paris

Tokyo

Bertrand Hochet Antonio J. Acosta
Manuel J. Bellido (Eds.)

Integrated Circuit Design

Power and Timing Modeling,
Optimization and Simulation

12th International Workshop, PATMOS 2002
Seville, Spain, September 11-13, 2002
Proceedings



Springer

Series Editors

Gerhard Goos, Karlsruhe University, Germany
Juris Hartmanis, Cornell University, NY, USA
Jan van Leeuwen, Utrecht University, The Netherlands

Volume Editors

Bertrand Hochet
Swiss University of Applied Science
Ecole d'Ingénieurs du Canton de Vaud
Microelectronics and Systems Institute, Digital Communications Team
Rue de Galilée 15, 1400 Yverdon, Switzerland
E-mail: bertrand.hochet@eivd.ch

Antonio J. Acosta
Manuel J. Bellido
Universidad de Sevilla
Instituto de Microelectrónica de Sevilla-CNM-CSIC
Departamento do Diseño Digital
Departamento de Electrónica y Electromagnetismo
Departamento de Tecnología Electrónica
Avda. Reina Mercedes, s/n. Edif. CICA
E-mail: {acojim, bellido}@imse.cnm.es

Cataloging-in-Publication Data applied for

Die Deutsche Bibliothek - CIP-Einheitsaufnahme

Integrated circuit design : power and timing modeling, optimization and simulation ; 12th international workshop ; proceedings / PATMOS 2002, Seville, Spain, September 11 - 13, 2002. Bertrand Hochet ... (ed.). - Berlin ; Heidelberg ; New York ; Barcelona ; Hong Kong ; London ; Milan ; Paris ; Tokyo : Springer, 2002
(Lecture notes in computer science ; Vol. 2451)
ISBN 3-540-44143-3

CR Subject Classification (1998): B.7, B.8, C.1, C.4, B.2, B.6, J.6

ISSN 0302-9743

ISBN 3-540-44143-3 Springer-Verlag Berlin Heidelberg New York

This work is subject to copyright. All rights are reserved, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, re-use of illustrations, recitation, broadcasting, reproduction on microfilms or in any other way, and storage in data banks. Duplication of this publication or parts thereof is permitted only under the provisions of the German Copyright Law of September 9, 1965, in its current version, and permission for use must always be obtained from Springer-Verlag. Violations are liable for prosecution under the German Copyright Law.

Springer-Verlag Berlin Heidelberg New York,
a member of BertelsmannSpringer Science+Business Media GmbH

<http://www.springer.de>

© Springer-Verlag Berlin Heidelberg 2002
Printed in Germany

Typesetting: Camera-ready by author, data conversion by PTP-Berlin, Stefan Sossna e.K.
Printed on acid-free paper SPIN: 10871110 06/3142 5 4 3 2 1 0

Preface

The International Workshop on Power and Timing Modeling, Optimization, and Simulation PATMOS 2002, was the 12th in a series of international workshops previously held in several places in Europe.¹ PATMOS has over the years evolved into a well-established and outstanding series of open European events on power and timing aspects of integrated circuit design. The increased interest, especially in low-power design, has added further momentum to the interest in this workshop. Despite its growth, the workshop can still be considered as a very focused conference, featuring high-level scientific presentations together with open discussions in a free and easy environment. This year, the workshop has been opened to both regular papers and poster presentations. The increasing number of worldwide high-quality submissions is a measure of the global interest of the international scientific community in the topics covered by PATMOS.

The objective of this workshop is to provide a forum to discuss and investigate the emerging problems in the design methodologies and CAD-tools for the new generation of IC technologies. A major emphasis of the technical program is on speed and low-power aspects with particular regard to modeling, characterization, design, and architectures. The technical program of PATMOS 2002 included nine sessions dedicated to most important and current topics on power and timing modeling, optimization, and simulation. The three invited talks try to give a global overview of the issues in low-power and/or high-performance circuit design. The first one presents a history of low-power clock watches, while the other ones deal with high performance clocking and the state of the art in low-voltage memories.

In 2002, the venue was Seville, Spain. The workshop was organized by the Microelectronics Spanish Center (IMSE-CNM) and the University of Seville. Seville is the major city in the southwest of Spain and one of its richest historic, cultural, and artistic spots. Seville is the capital of the Autonomous Community of Andalusia and has a population of over 700,000. Many very different cultures have figured in the history of Sevilla. The legacy of these cultures has grown over the centuries into the cultural, monumental, and artistic heritage that can be admired in the city's streets and museums today.

September 2002

Bertrand Hochet
Antonio J. Acosta
Jorge Juan-Chico

¹ Visit the web site: <http://www.patmos-conf.org>

Organization

Organization Committee

General Co-chairs:	Prof. Antonio J. Acosta Prof. Jorge Juan-Chico (Inst. de Microelectrónica de Sevilla, CNM; Universidad de Sevilla, Spain)
Program Chair:	Dr. Bertrand Hochet (Inst. of Microelectronics and Systems, University of Applied Sciences, Yverdon-les-Bains, Switzerland)

Local Committee

Finance Chair:	Prof. Manuel Valencia
Local Arrangements:	Prof. Carmen Baena Prof. Pilar Parra
Publication and Web:	Prof. Manuel Bellido Prof. Alejandro Millán Prof. Paulino Ruiz de Clavijo (Inst. de Microelectrónica de Sevilla, CNM; Universidad de Sevilla, Spain)

Program Committee

D. Auvergne (U. Montpellier, France)
J. Bormans (IMEC, Belgium)
J. Figueras (U. Catalunya, Spain)
C.E. Goutis (U. Patras, Greece)
A. Guyot (INPG Grenoble, France)
R. Hartenstein (U. Kaiserslautern, Germany)
S. Jones (U. Loughborough, UK)
P. Larsson-Edefors (U. Linköping, Sweden)
E. Macii (Politecnico di Torino, Italy)
V. Moshnyaga (U. Fukuoka, Japan)
W. Nebel (U. Oldenburg, Germany)
J.A. Nossek (T.U. Munich, Germany)
A. Núñez (U. Las Palmas, Spain)
M. Papaefthymiou (U. Michigan, USA)
H. Pfeiderer (U. Ulm, Germany)
C. Piguet (CSEM, Switzerland)

VIII Organization

R. Reis (U. Porto Alegre, Brazil)
M. Robert (U. Montpellier, France)
A. Rubio (U. Catalunya, Spain)
J. Sparsø (T.U. Denmark)
A. Stauffer (Swiss Fed. Inst. of Tech. Lausanne)
A. Stempkowski (Acad. of Sciences, Russia)
T. Stouraitis (U. Patras, Greece)
A.-M. Trullemans-Anckaert (U. Louvain)
R. Zafalon (STMicroelectronics, Italy)

PATMOS Steering Committee

Daniel Auvergne (U. Montpellier, France)
Reiner Hartenstein (U. Kaiserslautern, Germany)
Wolfgang Nebel (U. Oldenburg, Germany)
Christian Piguet (CSEM, Switzerland)
Antonio Rubio (U. Catalunya, Spain)
Joan Figueras (U. Catalunya, Spain)
Bruno Ricco (U. Bologna, Italy)
Dimitrios Soudris (U. Trace, Greece)
Jean Sparsø (T.U. Denmark)
Anne Marie Trullemans-Anckaert (U. Louvain, Belgium)
Peter Pirsch (U. Hannover, Germany)
Bertrand Hochet (EIVd, Switzerland)
Antonio J. Acosta (U. Sevilla/IMSE-CNM, Spain)
Jorge Juan (U. Sevilla/IMSE-CNM, Spain)
Enrico Macii (Politecnico di Torino, Italy)

Executive Subcommittee for 2002

President:	Christian Piguet (CSEM, Switzerland)
Vice-president:	Joan Figueras (U. Catalunya, Spain)
Secretary:	Reiner Hartenstein (U. Kaiserslautern, Germany)

Sponsoring Institutions

- IEEE Circuits and Systems Society
- IEEE Circuits and Systems Society Spanish Chapter
- European Commission, 5th Framework Programme, Grant IST2001-92074
- Consejo Superior de Investigaciones Científicas (CSIC), Centro Nacional de Microelectrónica

- Universidad de Sevilla, Vicerrectorados de Investigación y de Extensión Universitaria
- Ministerio de Ciencia y Tecnología, Plan Nacional de Investigación Científica, Desarrollo e Innovación Tecnológica, Acción especial TIC2001-4774-E
- Junta de Andalucía. III Plan Andaluz de Investigación

Table of Contents

Opening

The First Quartz Electronic Watch	1
<i>Christian Piguet (Centre Suisse d'Electronique et de Microtechnique SA, Neuchâtel, Switzerland)</i>	

Arithmetics

An Improved Power Macro-Model for Arithmetic Datapath Components . .	16
<i>D. Helms, E. Schmidt, A. Schulz, A. Stammermann, W. Nebel (OFFIS Research Institute, Oldenburg, Germany)</i>	
Performance Comparison of VLSI Adders Using Logical Effort	25
<i>Hoang Q. Dao, Vojin G. Oklobdzija (University of California, USA)</i>	
MDSP: A High-Performance Low-Power DSP Architecture	35
<i>F. Pessolano, J. Kessels, A. Peeters (Philips Research, Eindhoven, The Netherlands)</i>	

Low-Level Modeling and Characterization

Impact of Technology in Power-Grid-Induced Noise	45
<i>Juan-Antonio Carballo, Sani R. Nassif (IBM Austin Research Laboratory, USA)</i>	
Exploiting Metal Layer Characteristics for Low-Power Routing	55
<i>Armin Windschieggl, Paul Zuber, Walter Stechele (University of Tech- nology of Munich, Germany)</i>	
Crosstalk Measurement Technique for CMOS ICs	65
<i>F. Picot, P. Coll (ATMEL Rousset, France), D. Auvergne (Université de Montpellier, France)</i>	
Instrumentation Set-up for Instruction Level Power Modeling	71
<i>S. Nikolaidis, N. Kavvadias, P. Neofotistos, K. Kosmatopoulos, T. Laopoulos (Aristotle University of Thessaloniki, Greece), L. Bisdounis (INTRACOM S.A., Peania, Greece)</i>	

Asynchronous and Adiabatic Techniques

Low-Power Asynchronous A/D Conversion	81
<i>Emmanuel Allier, Laurent Fesquet, Marc Renaudin, Gilles Sicard (TIMA Laboratory, Grenoble, France)</i>	

XII Table of Contents

Optimal Two-Level Delay – Insensitive Implementation of Logic Functions	92
<i>Igor Lemberski, Mark Josephs (South Bank University, London, UK)</i>	
Resonant Multistage Charging of Dominant Capacitances	101
<i>Christoph Saas, Josef A. Nossek (Munich University of Technology, Germany)</i>	
A New Methodology to Design Low-Power Asynchronous Circuits	108
<i>Oscar Garnica, Juan Lanchares, Román Hermida (Universidad Complutense de Madrid, Spain)</i>	
Designing Carry Look-Ahead Adders with an Adiabatic Logic Standard-Cell Library	118
<i>Antonio Blotti, Maurizio Castellucci, Roberto Saletti (University of Pisa, Italy)</i>	

CAD Tools and Algorithms

Clocking and Clocked Storage Elements in Multi-GHz Environment	128
<i>Vojin G. Oklobdzija (University of California, USA)</i>	
Dual Supply Voltage Scaling in a Conventional Power-Driven Logic Synthesis Environment	146
<i>Torsten Mahnke, Walter Stechele (Technical University of Munich, Germany), Wolfgang Hoeld (National Semiconductor GmbH, Fuerstenfeldbruck, Germany)</i>	
Transistor Level Synthesis Dedicated to Fast I.P. Prototyping	156
<i>A. Landrault, L. Pellier, A. Richard, C. Jay (Infineon Technologies, Sophia Antipolis, France), M. Robert, D. Auvergne (LIRMM, Montpellier, France)</i>	
Robust SAT-Based Search Algorithm for Leakage Power Reduction	167
<i>Fadi A. Aloul (University of Michigan, USA), Soha Hassoun (Tufts University, USA), Kareem A. Sakallah, David Blaauw (University of Michigan, USA)</i>	

Timing

PA-ZSA (Power-Aware Zero-Slack Algorithm): A Graph-Based Timing Analysis for Ultra-Low Power CMOS VLSI	178
<i>Kyu-won Choi, Abhijit Chatterjee (Georgia Institute of Technology, Atlanta, USA)</i>	

A New Methodology for Efficient Synchronization of RNS-Based VLSI Systems	188
<i>Daniel González, Antonio García (Universidad de Granada, Spain), Graham A. Jullien (University of Calgary, Canada), Javier Ramírez, Luis Parrilla, Antonio Lloris (Universidad de Granada, Spain)</i>	

Clock Distribution Network Optimization under Self-Heating and Timing Constraints	198
<i>M.R. Casu, M. Graziano, G. Maserà, G. Piccinini, M.M. Prono, M. Zamboni (Politecnico di Torino, Italy)</i>	

A Technique to Generate CMOS VLSI Flip-Flops Based on Differential Latches	209
<i>Raúl Jiménez, Pilar Parra, Pedro Sanmartín, Antonio Acosta (Instituto de Microelectrónica de Sevilla, Spain)</i>	

Gate-Level Modeling

A Compact Charge-Based Propagation Delay Model for Submicronic CMOS Buffers	219
<i>José Luis Rossello, Jaume Segura (Balearic Islands University, Spain)</i>	

Output Waveform Evaluation of Basic Pass Transistor Structure	229
<i>S. Nikolaidis, H. Pournara (University of Thessaloniki, Greece), A. Chatzigeorgiou (University of Macedonia, Thessaloniki, Greece)</i>	

An Approach to Energy Consumption Modeling in RC Ladder Circuits ...	239
<i>M. Alioto (Università di Siena, Italy), G. Palumbo, M. Poli (Università di Catania, Italy)</i>	

Structure Independent Representation of Output Transition Time for CMOS Library	247
<i>P. Maurine, N. Azemard, D. Auvergne (University of Montpellier, France)</i>	

Memory Optimization

A Low Energy Clustered Instruction Memory Hierarchy for Long Instruction Word Processors	258
<i>Murali Jayapala, Francisco Barat, Pieter Op de Beeck (ESAT/ACCA, Heverlee, Belgium), Francky Catthoor (IMEC vzw, Heverlee, Belgium), Geert Deconinck, Henk Corporaal (Delft University of Technology, The Netherlands)</i>	

XIV Table of Contents

Design and Realization of a Low Power Register File Using Energy Model	268
<i>Xue-mei Zhao, Yi-zheng Ye (Harbin Institute of Technology, P.R. China)</i>	
Register File Energy Reduction by Operand Data Reuse	278
<i>Hiroshi Takamura, Koji Inoue, Vasily G. Moshnyaga (Fukuoka University, Japan)</i>	
Energy-Efficient Design of the Reorder Buffer	289
<i>Dmitry Ponomarev, Gurhan Kucuk, Kanad Ghose (State University of New York, USA)</i>	

High-Level Modeling and Design

Trends in Ultralow-Voltage RAM Technology	300
<i>Kiyoo Itoh (Central Research Laboratory, Hitachi Ltd., Tokyo, Japan)</i>	
Offline Data Profiling Techniques to Enhance Memory Compression in Embedded Systems	314
<i>Luca Benini (Università di Bologna, Italy), Alberto Macii, Enrico Macii (Politecnico di Torino, Italy)</i>	
Performance and Power Comparative Study of Discrete Wavelet Transform on Programmable Processors	323
<i>N.D. Zervas, G. Pagkless (Alma Technologies S.A., Attica, Greece), M. Dasigenis, D. Soudris (Democritus University of Thrace, Greece)</i>	
Power Consumption Estimation of a C Program for Data-Intensive Applications	332
<i>Eric Senn, Nathalie Julien, Johann Laurent, Eric Martin (University of South-Brittany, France)</i>	

Communications Modeling and Activity Reduction

A Low Overhead Auto-Optimizing Bus Encoding Scheme for Low Power Data Transmission	342
<i>Claudia Kretschmar, Robert Siegmund, Dietmar Müller (Chemnitz University of Technology, Germany)</i>	
Measurement of the Switching Activity of CMOS Digital Circuits at the Gate Level	353
<i>C. Baena, J. Juan-Chico, M.J. Bellido, P. Ruiz de Clavijo, C.J. Jiménez, M. Valencia (Instituto de Microelectrónica de Sevilla, Spain)</i>	

Low-Power FSMs in FPGA: Encoding Alternatives	363
<i>G. Sutter, E. Todorovich (Universidad Nacional del Centro, Tandil, Argentina), S. Lopez-Buedo, E. Boemo (Universidad Autónoma de Madrid, Spain)</i>	
Synthetic Generation of Events for Address-Event-Representation Communications	371
<i>Alejandro Linares-Barranco, Gabriel Jiménez, Antón Cívot (Universidad de Sevilla, Spain), Bernabé Linares-Barranco (Instituto de Microelectrónica de Sevilla, Spain)</i>	
Posters	
Reducing Energy Consumption via Low-Cost Value Prediction	380
<i>Toshinori Sato, Itsujiro Arita (Kyushu Institute of Technology, Japan)</i>	
Dynamic Voltage Scheduling for Real Time Asynchronous Systems	390
<i>Mohammed Es Salhiene, Laurent Fesquet, Marc Renaudin (TIMA Laboratory, Grenoble, France)</i>	
Efficient and Fast Current Curve Estimation of CMOS Digital Circuits at the Logic Level	400
<i>Paulino Ruiz-de-Clavijo, Jorge Juan, Manuel J. Bellido, Alejandro Millán, David Guerrero (Instituto de Microelectrónica de Sevilla, Spain)</i>	
Power Efficient Vector Quantization Design Using Pixel Truncation	409
<i>Kostas Masselos, Panagiotis Merakos, Costas E. Goutis (University of Patras, Greece)</i>	
Minimizing Spurious Switching Activities in CMOS Circuits	419
<i>Artur Wróblewski, Florian Auernhammer, Josef A. Nossek (Munich University of Technology, Germany)</i>	
Modeling Propagation Delay of MUX, XOR, and D-Latch Source-Coupled Logic Gates	429
<i>M. Alioto (Università di Siena, Italy), G. Palumbo (Università di Catania, Italy)</i>	
Operating Region Modelling and Timing Analysis of CMOS Gates Driving Transmission Lines	438
<i>Gregorio Cappuccino, Giuseppe Cocorullo (University of Calabria, Italy)</i>	
Selective Clock-Gating for Low Power/Low Noise Synchronous Counters 1	448
<i>Pilar Parra, Antonio Acosta, Manuel Valencia (Instituto de Microelectrónica de Sevilla, Spain)</i>	

XVI Table of Contents

Probabilistic Power Estimation for Digital Signal Processing Architectures	458
<i>Achim Freimann (Universität Hannover, Germany)</i>	
Modeling of Propagation Delay of a First Order Circuit with a Ramp Input	468
<i>Rosario Mita, Gaetano Palumbo (University of Catania, Italy)</i>	
Characterization of Normal Propagation Delay for Delay Degradation Model (DDM)	477
<i>Alejandro Millán, Jorge Juan, Manuel J. Bellido, Paulino Ruiz-de-Clavijo, David Guerrero (Instituto de Microelectrónica de Sevilla, Spain)</i>	
Automated Design Methodology for CMOS Analog Circuit Blocks in Complex Systems	487
<i>Razvan Ionita (Polytechnic Institute, Bucharest, Romania), Andrei Vladimirescu (University of California, USA), Paul Jespers (Universite Catholique de Louvain, Belgium)</i>	
Author Index	495