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Compact Models and Measurement Techniques for High-Speed Interconnects

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There is something fascinating about science. One gets such wholesale returns of conjecture out of such a trifling investment of fact.

Mark Twain

Foreword

High-speed interconnect analysis and design has been the focus of multi-disciplinary research activities involving new materials, structures and components. Interconnect performance can be a major design bottleneck in overall system performance, as described by researchers for nearly three decades. Research has led to technological breakthroughs in interconnect design and structures which paralleled transistor scaling and enabled system growth. The Georgia Institute of Technology has been one of the institutions where interconnect and packaging research has been a focus. Georgia Tech is the home of the longest running, externally funded center of excellence in high-speed interconnect, namely the Interconnect Focus Center (IFC), one of six focus centers sponsored by the semiconductor industry and DARPA through the Semiconductor Research Corporation. The IFC undertakes pioneering research work in electrical, optical and carbon interconnects.

The design of chip-to-chip interconnect is an area which needs increased attention due to the challenges in off-chip bandwidth and energy consumption. High frequency signal losses and bandwidth requirements, as outlined by the projections in the International Technology Roadmap for Semiconductors, give a description of the simultaneous need to reduce interconnect dimension, increase the data rate, and lower the energy consumed. This set of goals present challenges for device fabrication and characterization, which require development of complex analytical models, time-intensive simulations and state-of-the-art measurements. However, there are few sources available in the literature that exclusively discuss chip-to-chip interconnect. To this end, I feel the present text offers valuable insights for readers interested in this area of research and development. The authors have put forward a unified analytical modeling approach specifically for the analysis of chip-to-chip planar interconnects. In my view, this is an important first step toward the analysis and optimization of complex interconnect layouts governed by material and performance constraints. The inclusion of measurement and simulation as a part of the text would provide a holistic understanding of the subject matter to the readers.

This book is the outcome of on-going research by the Georgia Tech authors and is supported by research funding, such as provided by the IFC. Researchers here and throughout the world will hopefully find this book instrumental in advancing product design and analysis. This book takes the reader from a simple introduction to this area of research to a complete understanding of the modeling and measurement techniques. I congratulate the authors for their efforts in bringing this book to fruition and for contributing to the IFC advances at Georgia Tech.

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Preface

High-speed interconnects are essentially wires that form the media for transmission of analog and digital signals in electronic circuits and systems. Along with devices, these interconnects form a dense and complex fabric that is responsible for performance of integrated circuits, boards and packages. Signal integrity in high-speed interconnects is one of the most important design aspects for achieving high performance and throughput. For most of the early *IC* era, designers and practicing engineers focused on device improvement alone. While computational capability of devices is important, overall system performance will hit a plateau level if the performance of interconnects is not improved. With increased clock speeds and reduced aspect ratios, interconnects became the most crucial design bottleneck. This led to unprecedented thrust on the design and analysis of interconnects, both in the semiconductor industry as well in academia. Over the years it has become a major research theme in the *ITRS* predictions as well as several industrial and academic journals and conferences.

This book will provide a detailed analysis of issues related to high-speed interconnects from the perspective of modeling approaches and measurement techniques. In that we restrict ourselves to electrical chip-chip interconnects. Particular focus is laid on the unified approach (variational method combined with the transverse transmission line technique) to develop efficient compact models for planar interconnects. This book will give a qualitative summary of the various reported modeling techniques and approaches and will help researchers and graduate students with deeper insights into interconnect models in particular and interconnect in general. Time domain and frequency domain measurement techniques and simulation methodology are also explained in this book.

The book is organized into four chapters. Chapter 1 discusses the evolution of interconnects as a research theme from a historical perspective. From the simplistic lumped *RC* regime to more complex transmission line models, interconnect modeling has truly come of age. The importance of high-speed effects and its relevance to signal integrity is covered in this chapter. A brief historical outlook on interconnects starting from the early *RC* era is provided. Brief overviews of the technological evolution of interconnect technology and its influence on modeling

approaches is presented. However, for well-informed readers, having a glance at this introductory chapter should be sufficient. Chapter 2 explains the basics of compact model development for interconnects. We qualitatively summarize some of the most widely used analytical approaches toward analyzing transmission line interconnects. The chapter also presents the unified approach which is essentially a combination of variational analysis and transverse transmission line technique. The merit of this approach and its applicability is clearly explained to the readers. Application of the unified approach to develop compact physical models for high-speed interconnects is explained in Chap. 3. Models for parasitic extraction, computation of line impedance and time domain analysis of high-speed interconnects are explained. While the discussion is limited to a few useful interconnect structures it is felt that readers should be able to apply the technique to a wide variety of interconnect geometries. In Chap. 4, we discuss measurement techniques, wherein time domain and frequency domain measurement techniques are presented. Simulation methodology and numerical modeling approach for interconnects are also presented briefly.

This book will serve as a platform for the basic understanding of compact interconnect models using the unified approach. It also clearly explains measurement techniques and simulation methodologies for chip-chip interconnects to researchers and graduate students alike. As a note, this book is not a text book but will rather best fit as a reference book for students who are initiated to the area of interconnect modeling and measurements.

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Acknowledgments

Contents

Acronyms

ITRS	International technology roadmap for semiconductors
IC	Integrated circuits
CAD	Computer aided design
NoC	Network on chip
SoC	System on chip
TSV	Through silicon via
PCB	Printed circuit board
TEM	Transverse electromagnetic
EM	Electromagnetic
PEEC	Partial element equivalent circuit
MIC	Microwave integrated circuits
MMIC	Monolithic microwave integrated circuits
MCM	Multichip module
ISM	Industrial, scientific and medical
DVC	Discrete variational conformal
SPICE	Simulation program for integrated circuit environment
FDTD	Finite difference time domain
FEM	Finite element method
MoM	Method of moment
TDR	Time domain reflectometry
TDT	Time domain transmission
FDR	Frequency domain reflectometry
IFFT	Inverse fast fourier transform
TRL	Thru' reflect line
VNA	Vector network analyzer

Symbols

λ	Wavelength
G	Green's function
Y	Admittance parameter
Z, Z_0	Impedance parameter
C	Capacitance
Q	Charge
W_e	Electrostatic energy
V	Electric potential
I_S	Intensity of current source
N	Number count
φ	Potential function
ρ	Charge distribution
$f(x)$	Trial function
w	Line width
t	Line thickness
c	Wall to wall spacing
b_i	Height of the ith dielectric layer
ε_i	Permittivity of the ith dielectric layer
l	Length of the interconnect line
t	Thickness of the interconnect line
f	Frequency
d	Spacing between the interconnect line and the adjacent ground tracks
C_{Lower}	Capacitance per unit length of the region below the charge plane
C_{Upper}	Capacitance per unit length of the region above the charge plane
c'	Wall to wall spacing in the lower region
C_a	Line capacitance per unit length with dielectric replaced by air
L	Inductance per unit length of the interconnect line
v^a	Velocity of propagation

R	Resistance per unit length
ζ	Damping factor
t_d	50% delay time
t_r	90% rise time
t_o	Maximum/minimum overshoot time
t_s	Settling time
$\%O$	Maximum/minimum Percentage overshoot time
w_s	Width of the ground plane aperture
s	Edge to edge spacing between coupled lines
d_l	Spacing between interconnect line and ground tracks
pp'	Imaginary plane
C_{even}	Even-mode capacitance
C_{odd}	Odd-mode capacitance
G	Wall to wall spacing
Y_{even}	Even mode admittance
Y_{odd}	Odd mode admittance
Z_{even}	Even mode impedance
Z_{odd}	Odd mode impedance
C_v	Voltage coupling coefficient
k_c	Capacitive coupling coefficient
k_l	Inductive coupling coefficient
Z_{in}	Input impedance
$S_{11}, S_{12}, S_{21}, S_{22}$	S-parameters
V_p	Phase velocity