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Analysis of Bridge Defects in STT-MRAM Cells Under Process Variations and a Robust DFT Technique for their Detection

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Abstract. Spin-Transfer-Torque Magnetic RAM (STT-MRAM) is a promising non-volatile memory technology due to its ultra-integration density capability, nanosecond speeds for reading and writing operations and CMOS/FinFET fabrication process compatibility. STT-MRAMs may be affected by manufacturing defects, which may be challenging to detect under process variations in deeply scaled semiconductor technologies. Because of this, the importance of test techniques to target defects in this emerging memory technology. In this work, an STT-MRAM bit-cell is presented with its states due to the magnetic orientation of the ferromagnetic layers. The read and write operations of an STT-MRAM cell, including the read and write circuits, are revised in the scope of this work. The write time definition for an STT-MRAM cell is also revised. A defect model is used to analyze the STT-MRAM cell under short defects in the presence of process variations. A Design-For-Test (DFT) circuit to detect short defects in the STT-MRAM cells is proposed. The proposed methodology is based on the observation that a short defect modifies the amplitude of the currents entering and leaving the memory cell. Hence, the current difference between the currents entering and leaving the memory cell is used to discriminate between good cells and defective cells. The proposed DFT circuitry is robust to process-induced parameters variations in the memory cell. In such a way, defects detection probabilities are increased, and a high-quality product can be guaranteed.

Keywords: STT-MRAM, Short defect, Test, Design-for-Test, FinFET

1 Introduction

Spin-Transfer-Torque Magnetic RAM (STT-MRAM) is an emerging non-volatile memory technology with high endurance and CMOS/FinFET compatibility [1]. STT-MRAM has attractive features such as non-volatility, which means that the stored information remains when the power supply is turned off, and high endurance, which means it is possible to write data for an unlimited number of times. STT-MRAM also provides zero standby leakage. The International Technology Roadmap for Semiconductor (ITRS) highlighted STT-MRAM as a promising candidate for future on-chip memory applications [2].

Like in other types of memories, the main operations carried out in STT-MRAM are the writing and reading operations. The correct behavior of an STT-MRAM may be impacted by manufacturing defects, which may affect the access transistor, the MTJ and the interconnections of the STT-MRAM cell. If the access transistor is fabricated with FinFET technology new defects like stuck-open fin or single open gate in multi-fin structures may affect it [3] [4] [5]. The MTJ device may be affected by different types of defects like a short on the insulator oxide [6], an open defect in any terminal and a stuck-at-AP/stuck-at-P faults [7]. Resistive shorts/opens may affect the interconnections in the STT-MRAM memory [8] [9]. Fault models based on defective memory behavior are usually developed for test purposes [9]. Fault models may be used for test pattern generation. Memory fault models are usually classified depending on the operation they affect, reading or writing operation, as shown in Fig. 1.

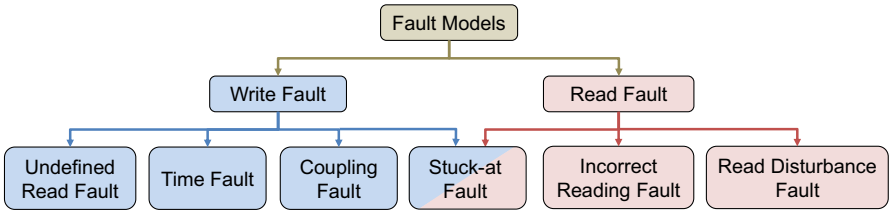


Fig. 1. STT-MRAM cell fault models

In a writing operation, an open resistive defect may reduce the current applied to the cell memory, and the cell may not change state. However, in an STT-RAM memory, the writing process has a probabilistic nature, so write failure also has the same nature, and it can not be known with certainty if the failure occurs always occur [10]. This fault is known as Undefined Write Fault (UWF) [11]. It is said that a Time Fault (TF) [9] occurs if the open resistive defect allows the current to be large enough to ensure that the desired state is written in the STT-MRAM cell, but it does not allow the memory cell to perform the writing process in a particular time. A short resistive defect may affect the gates of the access transistors in two STT-MRAM cells. The short defect is sensitized when trying to write a cell, and the access transistor is not completely turned on. As a consequence, the writing operation is not correctly performed. This fault is known as Coupling Fault (CF) [9]. An incorrect Reading Fault (IRF) [11] is said to occur when a resistive defect changes the measured voltage value of the cell in a read operation. A Read Disturbance Fault (RDF) [9] occurs when a short defect increases the current in a reading operation and change the value stored in STT-MRAM memory. In the Stuck-at Fault (SaF) a resistive short defect connects the internal node of the STT-MRAM cell with the power rails electrically, which causes malfunctions in both writing and reading operations

[11]. Recently, a novel generic defect modeling methodology that captures the non-linear behavior of the STT-MRAM has been proposed [12] .

Efficient defect test and diagnosis are critical to assure high-quality memory arrays, but this is a challenging task due to process-induced parameters variations, which may mask the impact of a defect on the functionality of the cell. The test approaches for digital integrated circuits can be categorized as fault-oriented or defect-oriented tests. In a fault-oriented test, the obtained logic result at the primary outputs is compared against the expected result. In a defect-oriented test approach, a parameter of the tested circuit (i.e., current consumption) is monitored to detect the presence of a defect. There is not required to observe the faulty logic behavior at main circuit outputs, which is a significant advantage. Thus, a defect-oriented test is more adequate for the detection of both strong and weak defects. In [13], a circuit-level approach to detect read disturbs faults was proposed. The circuit detects the change in the current through a cell when a read disturb fault occurs.

In this work, we propose a modified Design-For-Test (DFT) read circuit to detect resistive-short defects between an internal node of an STT-MRAM and an external node [14]. The proposed test circuit performs a defect-oriented test, which is adequate for the detection of weak defects that may escape to conventional logic test and degrade the memory block reliability [15]. The proposed test circuit is based on the observation that a short defect makes different the amplitude of the currents entering and leaving a memory cell. The DFT read circuitry can measure both the currents entering and leaving a memory cell. The proposed test technique provides higher defect detection and diagnosis capabilities. The capability of the proposed test circuit to detect resistive-short defects that can escape conventional logic test is validated under process variations effects, and it is shown that the defect detectability is improved. This chapter extends the analysis of the previous work and performs a comparative analysis between the conventional test techniques and the proposed DFT technique.

The rest of this chapter is organized as follows: Section 2 presents the operating principles of an STT-MRAM cell. Section 3 describes the read and write operation of the STT-MRAM cell with the read and write circuits used. In section 4, the writing time definition of an STT-MRAM cell is analyzed closely. Section 5 presents an analysis of the electrical behavior of the memory cell under the presence of resistive short defects. Section 6 presents the proposed test technique. Section 7 analyzes the cost of the proposed test technique, and a comparison between the proposed test technique and a conventional logic based test is made. Finally, Section 8 presents the conclusions of this work.

2 Memories Based on STT-MRAM

A single STT-MRAM memory is formed by a Magnetic Tunneling Junction (MTJ), which is a spintronic storage device, and an access transistor as illustrated in Fig. 2(a). The MTJ has two ferromagnetic layers separated by a very thin insulator [16]. The use of a FinFET transistor as the access device is pre-

ferred over a CMOS planar transistor due to its superior gate controllability, larger "ON" current, and lower variability. The magnetic orientation of the bottom layer, called Pinned Layer (PL), is fixed. However, the magnetic orientation of the top layer, called Free Layer (FL), is allowed to switch its magnetic orientation concerning the PL using a spin-polarized current through the MTJ. The electrical resistance of the device depends on the magnetic orientation of the two ferromagnetic layers (See Fig. 2(b)). A larger electrical resistance is observed when the magnetic orientations of the layers point in opposite directions (known as Anti-parallel state) compared to the state when the magnetic orientations of the layers point in the same direction (known as Parallel state) [17] [18]. This phenomenon is known as Giant Magneto Resistance [19] [20]. The low and high MTJ resistance states correspond to the logic 0 and 1 states, respectively.

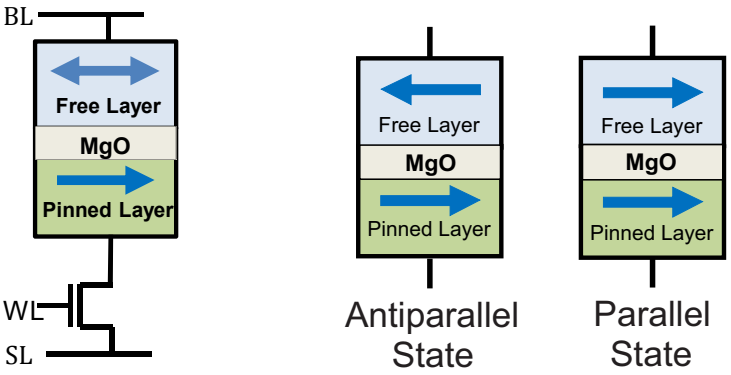
A data can be written into and read from the cell by applying appropriate voltages to bit-line (BL), source-line (SL) and Word-Line (WL) terminals of the cell (See Table 1). A current needs to flow from the BL to the SL terminals for writing a Parallel (P) state, which is accomplished by applying BL=VDD, and SL=0. On the other hand, a current needs to flow from the SL to the BL terminals for writing an Anti-Parallel Parallel (AP) state, which is accomplished by applying BL=0, and SL=VDD. The current that flows through the MTJ has to be large enough to switch the magnetization orientation of the free-layer [21] during a write operation successfully. In this way, the memory can change from anti-parallel state to parallel state ($AP \rightarrow P$) or vice-versa ($P \rightarrow AP$). It is important to mention that this current must be bidirectional to perform the change of state in both cases.

The read operation is performed by sensing the resistance of the MTJ. This is done by applying a small read current to the cell and comparing the voltage drop with a reference voltage. Unlike write operation that requires bi-directional current, the read operation only requires current flowing from BL to SL terminals. In the reading procedure, a lower current than the write current is applied at the cell, and the voltage at the cell is measured to identify its state [22].

Table 1. Signal conditions for write and read operations.

Node	**Write**		**Read**
	$AP \rightarrow P$	$P \rightarrow AP$	
WL	V_{DD}	V_{DD}	V_{DD}
BL	0	V_{DD}	V_{DD}
SL	V_{DD}	0	0

Table 2 shows some of the main MTJ parameters used in this work. Other parameters were settled as default in [23].



(a) STT-MRAM bit-cell

(b) MTJ in anti-parallel and paralell states

Fig. 2. STT-MRAM bit-cell and its states due to the magnetic orientation of the ferromagnetic layers.

Table 2. MTJ parameters

Parameter	Value
MTJ Size	$30nm \times 30nm \times 1.5nm$
Saturation Magnetization	$850emu/cm^3$
Energy Barrier	$56k_BT$
MgO thickness	1nm

3 Read and Write Operations of STT-MRAM Cells

Figure 3 illustrates a memory array architecture using the STT-MRAM cell. Memory cells are accessed by activating a word line (WL_i) and the pass transistors of the desired column. The access to the cells is defined by the word and column decoder circuitries. It should be noted that the number of selected columns depend on the required application. Figure 4 shows a single STT-MRAM cell with the used read and write circuits. The access transistor of the cell, which is driven by the word-line (WL) signal, controls whether current can flow through the MTJ to perform write and read operations.

3.1 Read Operation

The read circuit (See Fig. 4) is activated when the Read Enable signal is set at a high logic state (RE=1). A current I_{REF} is generated using a reference cell whose resistance is designed to be the average between the parallel (R_P) and anti-parallel (R_{AP}) resistances of the STT-MRAM cell $(R_P + R_{AP})/2)$. This

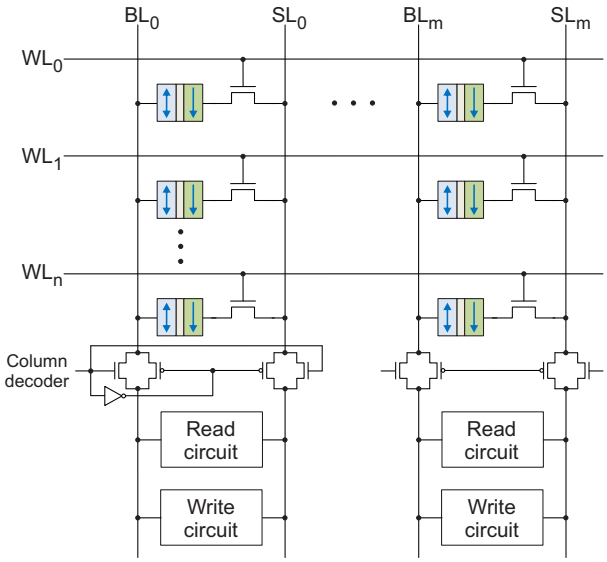


Fig. 3. Memory array using the STT-MRAM bit-cell.

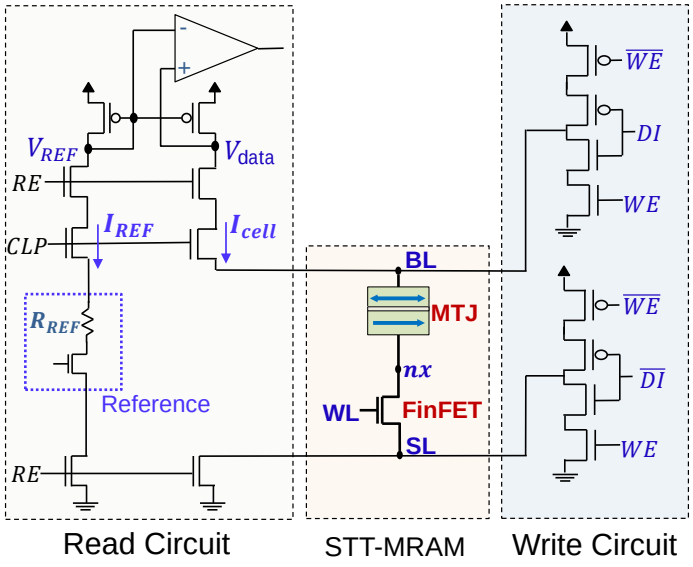


Fig. 4. STT-MRAM bit-cell with read and write circuits.

current is copied and applied to the memory cell to be read. The current I_{REF} generates a voltage V_{REF} at one end of the terminals of the current mirror, and the current I_{cell} generates a voltage V_{cell} at the other end terminal of the current

mirror. The voltages generated at the current mirror terminals (V_{REF}, V_{cell}) are not the same since the resistances of the STT-MRAM cell, and the reference cell are different. The voltage difference between V_{REF} and V_{cell} is measured using a sense amplifier to determine whether the STT-MRAM cell is in the P or AP state. The clamp voltage (CLP) is used to limit the amount of reading current (I_{REF}), so that unintentional writes do not occur.

3.2 Write Operation

The write circuit is activated when the Write Enable signal is set at a high logic state (WE=1). The direction of the current applied to the memory cell depends on the Data Input (DI) to be written. The AP state is written if $DI = 1$ while the parallel state is written if $DI = 0$. A current flows from SL to BL for $DI = 1$, and thus, an AP state is written in the MTJ. A current flows from BL to SL for $DI = 0$, and thus, a P state is written in the MTJ. The transistors of the writing circuit were made large enough to provide sufficient current capability for a correct write operation.

4 Write Time Definition for an STT-MRAM Cell

One of the major issues for proper operation of the STT-MRAM cell is that a sufficiently large current has to flow through the cell for a long enough time to perform a successful write operation. The required large current leads to a high write energy consumption. Energy efficiency is further degraded due to the required current asymmetry in the write operations [24]. Energy efficiency of the STT-MRAM has been addressed by carefully size optimization of the access transistor in [25]. The size of the access transistor is iteratively increased until the desired write time performance for the slow process corner is achieved. This Section closely analyzes the write time behavior when writing P and AP states.

In a conventional STT-MRAM cell, the latency time for each writing transition ($P \rightarrow AP$ or $AP \rightarrow P$) is different. This asymmetry is caused due to the different spin-transfer efficiency of each MTJ layer, which makes the current to switch the MTJ magnetization state different depending on the state to be written. Write time asymmetry also occurs due to source-degeneration of the access transistor during the $P \rightarrow AP$ write operation, which reduces the effective gate to source voltage of the NFET, and consequently, its current driving capability, resulting in larger write latency. Figure 5 shows the current waveform for the two write operations in an STT-MRAM cell. A FinFET access transistor with 2 Fins and 2 Fingers ($W_{eff} \sim 224nm$) was used. As can be observed, the write latency is determined by the $P \rightarrow AP$ operation where source degeneration occurs.

For writing a $P \rightarrow AP$ state (See Fig. 5), the current that initially flows through the cell is $130\mu A$, which makes the MTJ flip its magnetic orientation in $7.28ns$. Then, the current reduces to $76\mu A$ when the memory switches its state as the AP state has a higher resistance than the P state. For writing an $AP \rightarrow P$ state (See Fig. 5), the initial current is $142\mu A$. Note that although the MTJ is at

the high resistance state (AP), the access transistor does not experience source-degeneration for this transition. Therefore, the current that can flow at the beginning of this operation is larger than the current for the $P \rightarrow AP$ writing. The writing of the $AP \rightarrow P$ state takes $2.98ns$. Then, the current increases when the memory switches its state as the P state has a lower resistance than the AP state. Note that the current keeps flowing through the cell the slower $P \rightarrow AP$ transition defines the pulse current duration. This unnecessary current contributes to extra power dissipation and degrades the energy efficiency of the memory cell.

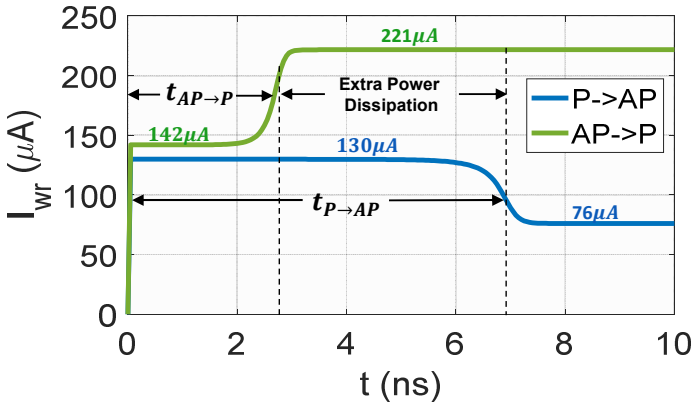


Fig. 5. Current waveforms for both $P \rightarrow AP$ and $AP \rightarrow P$ write operation.

STT-MRAM suffers from process variations on the access transistor and the MTJ. Process variations lead to variations in the write time of the cell because they affect the current drive capability of the access transistor as well as the magnetic and electric properties of the MTJ (i.e., MTJ resistance and critical switching currents). Due to process variations, the write delay distribution of the STT-MRAM cell has a long tail, which may degrade the memory yield [26], [27]. The size of the access transistor must be selected to compensate for the impact of process variations with an acceptable write failure probability.

5 Analysis of STT-MRAM Behavior Under Short Defects

Correct STT-MRAM behavior may be affected by manufacturing defects. A comprehensive analysis of all the possible defects in an STT-MRAM was presented in [9]. It was shown that due to the fundamental differences between classic SRAM and STT-MRAM, some fault models and test techniques used in SRAM are not extendable to STT-MRAM technology. Resistive short defects may alter the correct functionality of the cell. However, when the defects are

not strong enough, its detection becomes very difficult, and they may escape the post-manufacturing test, especially under the effect of process variations.

An STT-MRAM cell including the read and write circuits has been simulated. The design characteristics of the single memory and the set-up conditions for Spice simulations used from now on are given. The MTJ has dimensions of $60nm \times 40nm \times 1.4nm$. A stability factor of $\Delta = 70$ is considered. Other MTJ parameters are set as in [23]. A FinFET access transistor with 6 $fins$ was used to provide enough current capability to perform a successful write operation in $3.5ns$. A Predictive 20nm FinFET technology [28] is used along with the SPICE-compatible MTJ model proposed in [23]. Variations in the MTJ were assumed of 15% for the cross-sectional area (A_t) and 5% for the oxide barrier thickness (t_{ox}). For the access transistor, 30% of threshold voltage (V_{th}) variation due to the work function variation was assumed. For simplicity purposes, process parameters variations were only considered for the single memory cell.

5.1 Defect Model for Short Defects in the STT-MRAM

Figure 6 shows the used general defect model to analyze the behavior of the STT-MRAM under short defects. The resistance R_{VDD} considers those possible resistive-short defects between the internal node of the STT-MRAM cell and the power supply terminal, and the resistance R_{GND} considers those possible resistive-short defects between the internal node of the STT-MRAM cell and the ground terminal. R_{VDD} and R_{GND} represent the behavior of realistic short defects that occur between the internal node of the cell and power/ground terminals. However, the proposed methodology is also valid to detect other types of short defects as explained later in section 7.4.

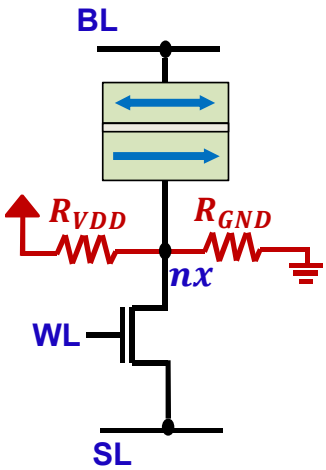


Fig. 6. STT-MRAM cell with resistive short defects.

5.2 Impact of Short Defects on Write Operation

The nominal current that flows through the MTJ (I_{MTJ}) during the writing process of a P and an AP states is shown in Figs. 7(a) and 7(b), respectively. The writing time (t_{wr}) to switch the magnetization orientation of the MTJ depends on the amplitude of the current that initially flows through the MTJ. For writing a parallel state (See Fig. 7(a)), the current that initially flows through a *"good"* cell is close to $145\mu A$. When a resistive defect R_{VDD} exists, the write time increases because this defect reduces the current that can flow through the MTJ since the access transistor has to drive both the MTJ current and the defect current. On the other hand, defect R_{GND} slightly reduces the write time because more current flows through the MTJ due to an additional conducting path to ground. For writing an anti-parallel state (See Fig. 7(b)), the current that flows through a *"good"* cell is close to $139\mu A$. A resistive defect R_{VDD} increases the current that flows through the MTJ, which reduces the write time. A resistive defect R_{GND} reduces the current that flows through the MTJ, which increases the write time.

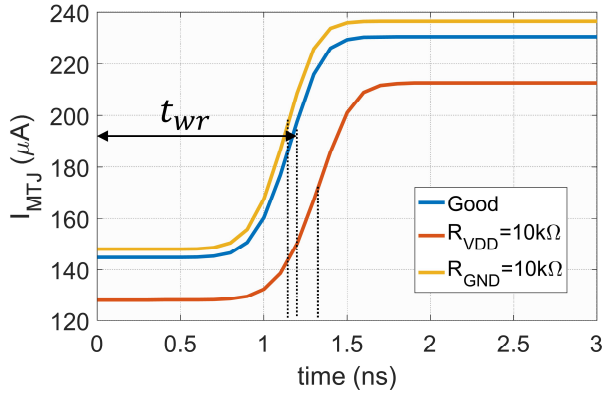
Impact of Process Variations

The write pulse duration constraint for the designed cell was of $3.5ns$. This write time value corresponds to the largest write time that the defect-free cell can take under process variations. 1000 Monte-Carlo simulations were made. Note that this write time value corresponds to the $P \rightarrow AP$ operation, which is slower than the $AP \rightarrow P$ operation due to source degeneration of the access transistor [24]. If the cell's write time becomes larger than $3.5ns$ due to a short defect, an incorrect write operation is performed, and the defect presence can be detected using a conventional logic-based test. A resistive defect value $2k\Omega$ has been considered for R_{VDD} and R_{GND}.

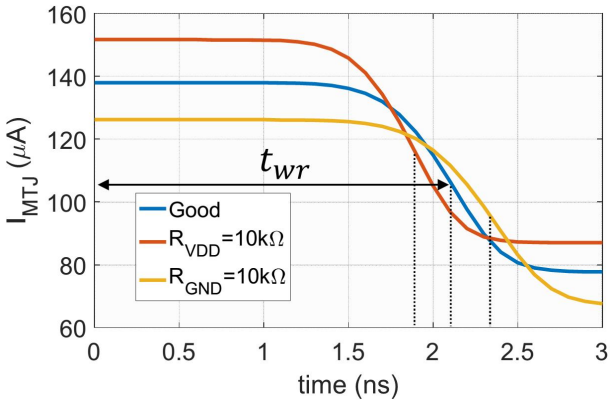
Write time histograms for the $AP \rightarrow P$ write operation for good and defective cells are shown in Fig. 8(a). R_{GND} moves the write time distribution to the left, and therefore, it does not cause a logic fault. R_{VDD} moves the write time distribution to the right, but most of the write time values does not cause a logic fault. It can be observed that most of the write time values are within the designed write time margin of the cell ($t_{wr} = 3.5ns$), and hence, they represent test escapes.

Write time histograms for the $P \rightarrow AP$ write operation for good, and defective cells are shown in Fig. 8(b). R_{VDD} moves the write time distribution to the left, and consequently, it does not trigger a logic fault. On the other hand, defect R_{GND} moves the write time distribution to the right. In this case, most of the write time values of the defective cell are larger than the designed write time margin of the cell ($t_{wr} = 3.5ns$), and hence, they can be detected using a logic-based test. However, some defective cells with write times smaller than the designed write time margin of the cell are not detected using a logic based test.

Figures 8(a) and 8(b) suggest that a conventional logic-base test using the write operation may fail to detect short defects related to R_{VDD}. Moreover, some short defects related to R_{GND} also may not be detected.



(a) $AP \rightarrow P$



(b) $P \rightarrow AP$

Fig. 7. Current waveforms for both $P \rightarrow AP$ and $AP \rightarrow P$ write transitions.

5.3 Impact of Short Defects on the Read Operation

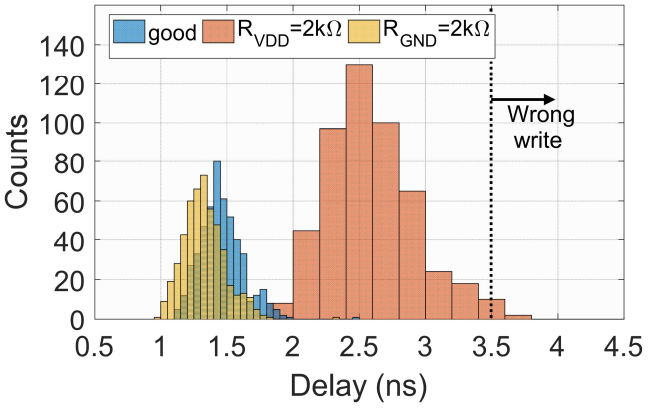
Figure 9 shows the voltage V_{cell} generated at the current mirror terminals in the read circuit (See Fig. 4) as a function of the short defect resistance for both R_{GND} and R_{VDD} defects. The black dashed lines correspond to the case of V_{cell} of a defect-free cell, where V_{cell} is $0.30V$ and $0.85V$ for the MTJ at the P and AP state, respectively. The voltage V_{REF} generated by the reference cell is $0.66V$.

A read error of the AP state is assumed for the following condition:

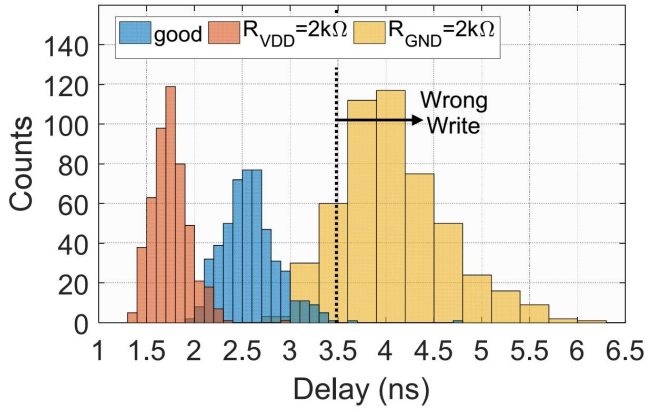
$$V_{cell} < V_{REF} \tag{1}$$

A read error of the P state is assumed for the following condition:

$$V_{cell} > V_{REF} \tag{2}$$



(a) $AP \rightarrow P$



(b) $P \rightarrow AP$

Fig. 8. Write time histograms for the good and defective cells.

Resistive defect R_{VDD} injects extra current to the internal node of the cell, which has to be driven by the access transistor. Because of this, the resistance seen from the BL node increases, and hence, the generated voltage V_{cell} increases. Figure 9 shows that no logic error appears for reading an AP state for the defect R_{VDD}. However, a logic error occurs in a small range of defect resistance values for reading a P state.

Defect R_{GND} is placed in parallel with the access transistor. When the resistance of the short defect is large, its effect on the overall cell resistance is negligible. When the resistance of the short defect is small, the equivalent resistance reduces until it becomes closer to the pure resistance of the MTJ. The generated voltage V_{cell} reduces as R_{GND} becomes smaller (See Fig. 9). Resistive defect R_{GND} defect does not trigger any incorrect read operations. Therefore, this defect can not be detected by a read operation using conventional logic test.

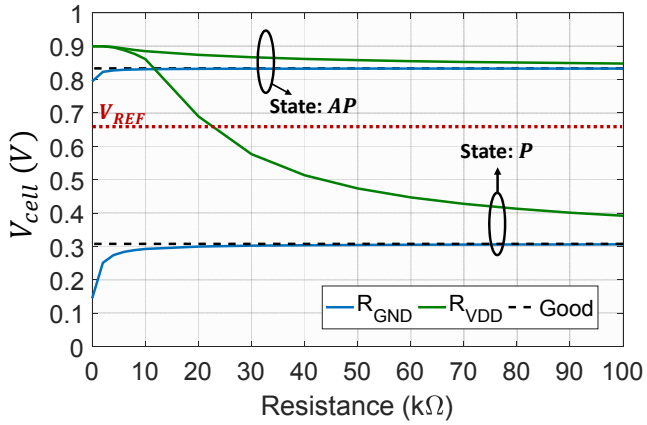


Fig. 9. Voltage generated by the memory cell (V_{cell} in Fig. 4) in a read operation as a function of the short defect resistance.

Impact of Process Variations

Figure 10 shows the histograms of the voltage V_{cell} for good and defective cells. A resistive shorts defect of $20k\Omega$ has been considered for R_{GND} and R_{VDD}. As expected, the defect R_{GND} does not trigger an incorrect read. Some of the defective cells with R_{VDD} may not cause an incorrect read (logic fault) and may escape the logic test.

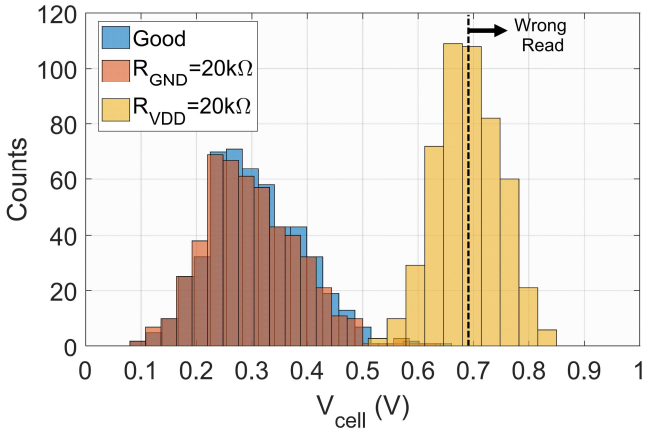


Fig. 10. Histogram of the voltage generated by the memory cell (V_{cell} in Fig. 4) in a P state read operation.

5.4 Summary Behavior of Write and Read Operation Under Short Defects

Table 3 shows the summary behavior of the read and write operations of a memory cell in the presence of resistive short defects. It can be observed that resistive short defect R_{GND} cannot be detected with a read operation, but they may be detected with a write operation for $P \rightarrow AP$ condition. Resistive short defect R_{VDD} presents poor detectability. Defect R_{VDD} is more difficult to be detected than defect R_{GND} using conventional write and read operations. Even more, the cell performance metrics as the write margin, read margin, and the MTJ resistance between the AP state and P state, called Tunneling Magnetoresistance Ratio (TMR), may be degraded due to the presence of defects. A higher TMR is desirable because it allows better discrimination between the AP state and the P state during the reading procedure [18] [12]. Figure 11 shows the behavior of the high-resistance state (R_{AP}), the low-resistance state (R_P) and cell TMR (CTMR) as a function of the resistance value of the short defect. It can be observed that the resistive defect modifies the values of $R_{AP}$and R_P, and as a consequence, the cell TMR. Lower TMR values affect sense margin, and they may pose a reliability concern.

Table 3. Summary behavior of write and read operation under short defects

Defect	Write		Read	
	$AP \rightarrow P$	$P \rightarrow AP$	AP	P
R_{GND}	NO	YES	NO	NO
R_{VDD}	Poor	NO	NO	Poor

6 Proposed Test Technique

6.1 Fundamental of the Proposed Test Technique

The proposed test technique is based on the observation that a resistive-short defect between an external node and the internal node of the memory cell modifies the current flowing into (through BL terminal) and out (through SL terminal) of the cell. As shown in Fig. 12(a), a good cell behaves as a single current path, where the current provided by the read circuitry at BL terminal flows through the MTJ and the access transistor to the SL terminal. In the presence of a short defect R_{VDD} (See Fig. 12(b)), current is injected into the cell (I_{short}), and hence, I_{SL} becomes greater than I_{BL}. Similarly, in the presence of a R_{GND} short (See Fig. 12(c)), the current is removed from the cell (I_{short}), and hence, I_{BL} becomes greater than I_{SL}.

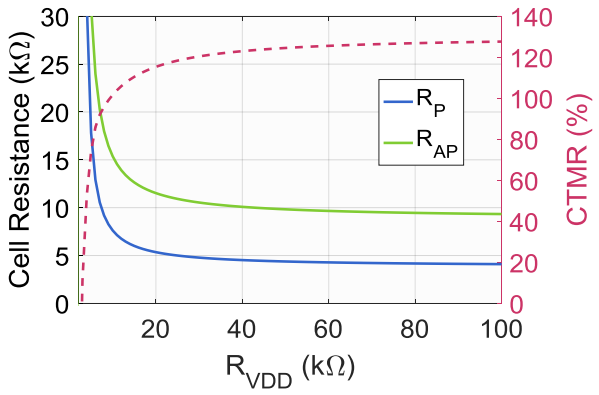


Fig. 11. Impact of the resistance value of the short defect on the Cell TMR.

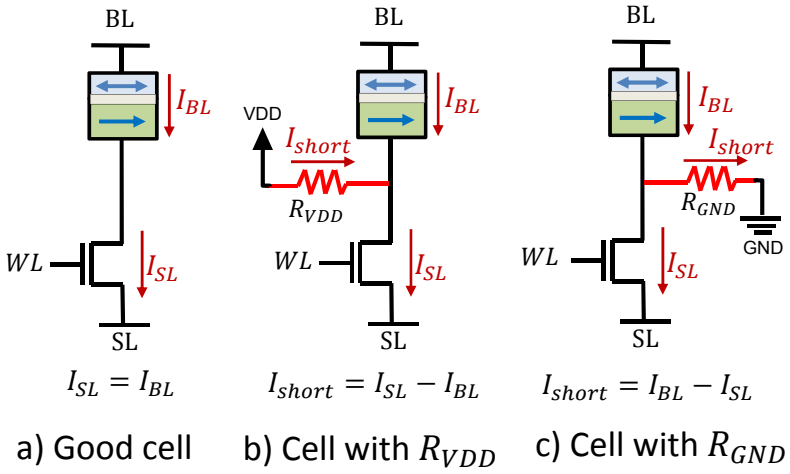
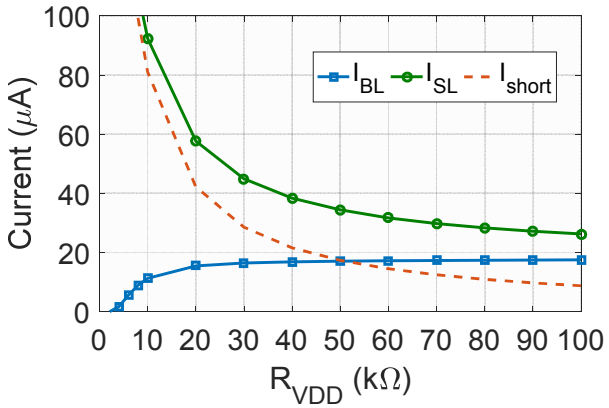


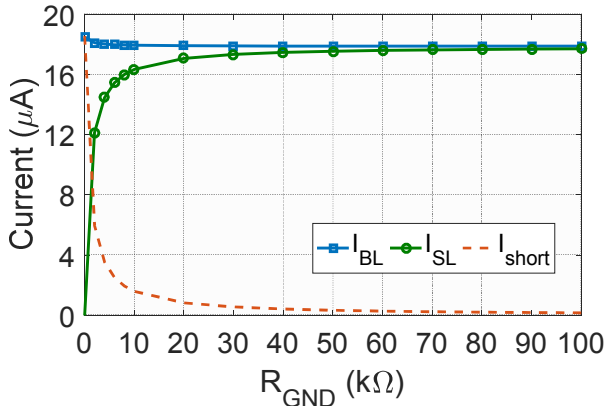
Fig. 12. Current paths in defect-free and defective STT-MRAM cells.

Figures 13(a) and 13(b) show the currents flowing through BL (I_{BL}) and SL (I_{SL}) terminals and also the current flowing through the short defect (I_{short}). These currents are plotted as a function of the resistance values of R_{VDD} and R_{GND} for a read operation. It can be observed that the currents in the terminals SL (I_{SL}) and BL (I_{BL}) have different behavior. This is due to the existence of an alternative conducting in the presence of the resistive short defect. Another important observation is that the current difference between I_{SL} and I_{BL} is more significant for lower resistance values of the short defect. The current difference between I_{SL} and I_{BL} indicates that monitoring the current difference between I_{SL} and I_{BL} is more effective than monitoring only a single current value. Resistive defect R_{VDD} causes a more significant current difference than the defect

R_{GND} (See Figs. 13(a) and 13(b)). Hence, defect R_{VDD} would present better detectability than defect R_{GND} with our proposed test methodology.



(a) R_{VDD}

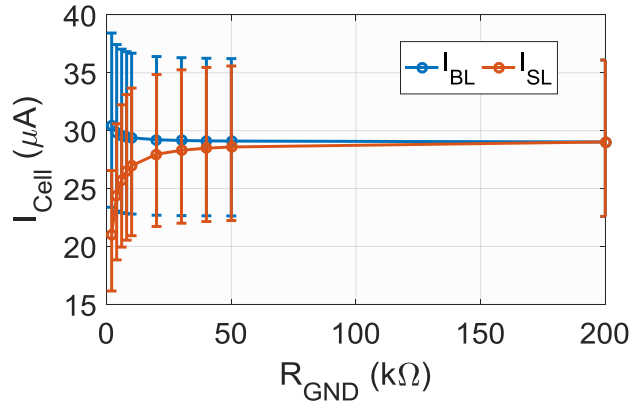


(b) R_{GND}

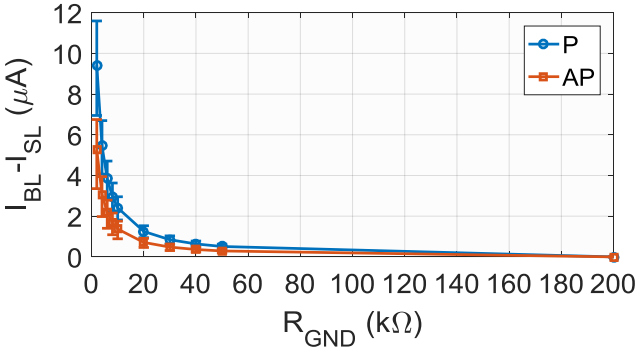
Fig. 13. Behavior of BL and SL currents as function of the short defect resistance.

Figure 14 illustrates the benefits of our proposal under the effect of process variations for resistive defect R_{GND}, which present lower current values. Figure 14(a) shows the single values of the currents I_{BL} and I_{SL} under process variations. It can be observed that the single current values go up and down from the nominal value, which makes difficult to discriminate good circuits from bad circuits sensing only one of these currents. Figure 14(b) b shows the current difference values between the currents I_{BL} and I_{SL} under process variations. It can be observed that the current difference values increase following a mono-

tonic trend as the resistive defect values decreases. This behavior of the current difference allows distinguishing good circuits from bad circuits.



(a) Single current monitoring under process variations



(b) Difference current monitoring under process variations

Fig. 14. Comparison between monitoring single and current difference under process variations.

6.2 Proposed Test Circuitry

In this Section, a DFT circuit oriented to defect detection without observability capability of the logic faulty behavior at main circuit outputs is proposed. This approach is adequate for the detection of weak defects, which are difficult to detect with a test based on classic logic fault observation. The benefit of the proposed test circuit to detect short defects sizes that can escape conventional logic test is validated under process variations effects. Therefore, the proposed

test technique is able to detect those weak short defects that do not cause a faulty behavior, but limiting the quality and lifetime of the entire memory block.

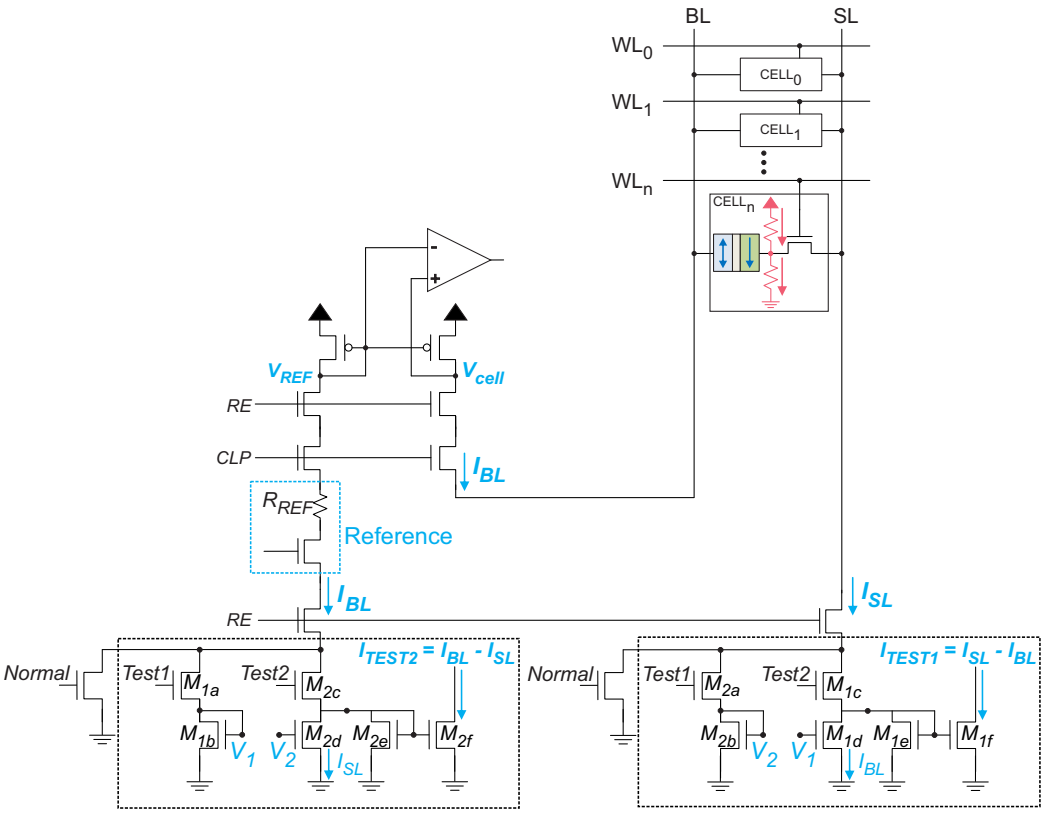


Fig. 15. Modified read circuit with test capability.

Figure 15 shows the proposed modified readout circuit with test capability based on the previous observation that a resistive short defect between an external node and the internal node of the memory cell modifies the current flowing into and out of the cell. The modified read circuit measures the difference between the current flowing into and out of the cell in the column. A significant current difference indicates the presence of a defect. Differential current amplifiers are introduced at both sides of the column (BL and SL). The modified read circuit has three possible operation modes: 1) Normal mode, 2) Test 1, and 3) Test 2 (See Fig. 15).

The mode Normal is activated by setting the signals $Normal = 1$ and *Test 1=Test 2=0*. Under these conditions, the normal functionality of the read circuit is obtained. The mode Test 1 is activated by setting the signals *"Test 1=1"* and

Normal=Test 2=0. In mode Test 1, the reference current (I_{REF}) passes through transistors M_{1a} and M_{1b} generating a voltage $V1$, which is used to copy I_{REF} to transistor M_{1d}. Note that $I_{REF} \approx I_{BL}$, thus the copied current represents I_{BL}. Since I_{SL} flows through M_{1c}, the current difference $I_{TEST,1} = I_{SL} - I_{BL}$ flows through transistor M_{1e}. This current is copied to M_{1f} which is the output transistor of the differential current amplifier. In other words, in mode Test 1 the operation $I_{TEST,1} = I_{SL} - I_{BL}$ is performed to generate an output current when I_{SL} is bigger than I_{BL}. Hence, possible resistive R_{GND} shorts defects are tested in mode Test 1. The mode Test 2 is activated by setting the signals *"Test 2=1"* and *Normal=Test 1=0*. The operation of mode Test 2 is very similar to mode Test 1, but in this case, the operation $I_{TEST,2} = I_{BL} - I_{SL}$ is performed to generate an output current at M_{2f} when I_{BL} is greater than I_{SL}. Hence, possible resistive R_{VDD} shorts defects are tested in mode Test 2.

The detection capability of the proposed circuit has been analyzed under the effect of process variations. Figures 16(a) and 16(b) show histograms of the current difference between BL and SL at the output of the proposed test circuit for both operation modes Test 1 and Test 2, respectively. 1000 Montecarlo simulations were run. Figure 16(a) shows that for strong resistive defects (smaller resistance), the test output current difference is more significant making easier the detection of the defect. Defective cells with weak short R_{VDD} as large as $100k\Omega$ can be fully distinguished from good cells as there is no overlap between the distribution of the defective cell and the good one. Defect R_{GND} is more difficult to detect. For defect $R_{GND} = 100k\Omega$, there is still a significant overlap between the current distribution of a good cell and the defective cell. However, resistive short defects of $20k\Omega$ can be fully detectable, which is still a significant improvement of the detection capability compared to the logic test.

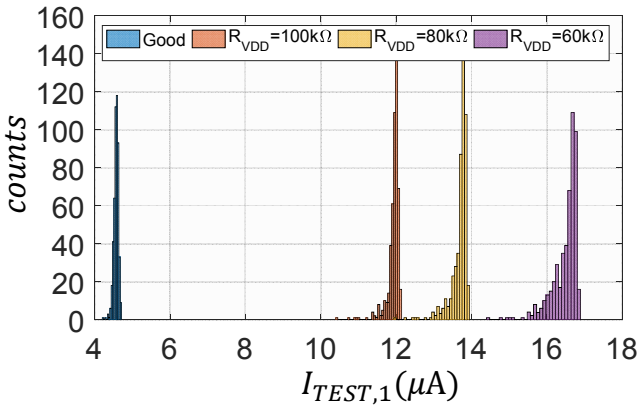
The obtained results show that the proposed DFT test circuit is capable of detected the resistive short defects with sizes that are not detectable using a conventional logic test. Moreover, the proposed test circuit could be used to diagnose the severity of a short defect by defining thresholds in the current difference.

7 Cost and Comparison of Our Proposal with Logic Test

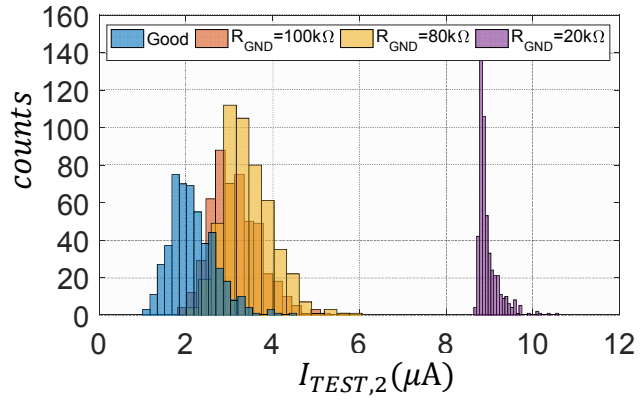
7.1 Detection Probability Comparison

Figures 17 and 18 shows the value of the detection probability (P_{det}) of short defects as a function of its resistance value for conventional test techniques (write and read operations test) and the proposed current difference test technique. 500 Monte Carlo simulations are done for each resistance value of the short defect. The Detection Probability (P_{det}) is computed with (3), where N_f is the number of runs presenting a fault and N_{MC} is the total number of Monte Carlo simulations.

$$P_{det} = \frac{N_f}{M_{MC}} \tag{3}$$



(a) Short R_{VDD} (Test Mode 1)



(b) Short R_{GND} (Test Mode 2)

Fig. 16. Current difference histograms for good and defective cells.

The largest write time ($P \rightarrow AP$) including process variations has been considered for a write fault to occur. A write fault occurs when the write time of the defective cell is greater than $3.5ns$. A read fault occurs when the V_{cell} is lower (higher) than $V_{ref} = 0.66V$ for P state (AP state). The detection thresholds of the proposed test technique are obtained from the histograms of the defect-free currents. A resistive short defect is assumed detectable when the current difference is higher than the maximum defect-free current from the histogram. The detection threshold current is $4.6\mu A$ for $I_{TEST,1}$ and $4.0\mu A$ for $I_{TEST,2}$.

For the R_{VDD} defect (See Fig. 17), a conventional write test detects the defect in the range from 0 to $1k\Omega$. The defect is not detectable using a conventional read operation when the cell has stored an AP state ($P_{det} = 0$), but when the cell has stored a P state the defect is detectable in the range from 0 to $200k\Omega$. The proposed test technique increases the detection range of this defect in two

orders of magnitude concerning the test based in the read operation when the cell has stored at P state. With the proposed DFT technique the R_{VDD} defects with values up to $1M\Omega$ are fully detectable and partially detectable at the range from $1M\Omega$ to $10M\Omega$.

On the other hand, the R_{GND} defect presents a lower detection range than the R_{VDD} defect (See Fig. 18). This defect can not be detected with a test based in the cell read operation, ($P_{det} = 0$ for both states). However, with a conventional test during the write operation, R_{GND} defects with values up to $1k\Omega$ are fully detectable and partially detectable in the range from $1k\Omega$ to $10k\Omega$. The proposed DFT technique fully detect the R_{GND} defect in a range from 0Ω to $40k\Omega$ and partially detects this defect in a range from $40k\Omega$ and $100k\Omega$.

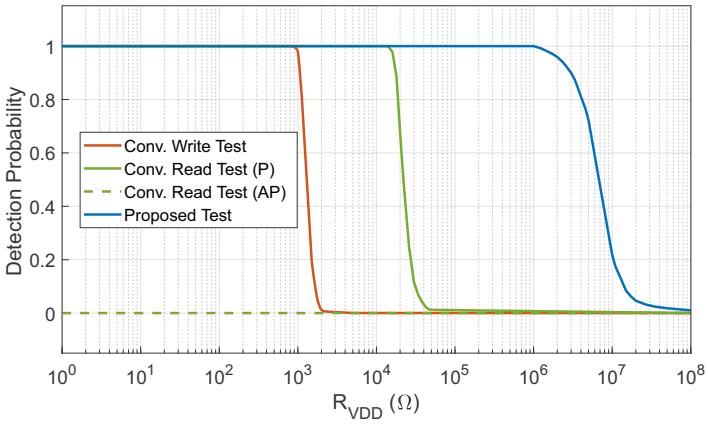


Fig. 17. Detection Probability for R_{VDD} short.

7.2 Hardware Comparison

A conventional test based in write and read operation does not present area overhead. Our proposal requires to include additional transistors and test control signals. The total area of the channels of all the transistors is used as an estimation on the area overhead of the proposed DFT technique. The area of the access transistor of each memory cell is taken into account. It is assumed that the MTJ does not impact the area as is located above the access transistor. It is important to emphasize that the transistors used to copy currents in the DFT circuit have a longer channel length to ensure a correct copy of the currents. For a column composed of 2kbit, the DFT read circuit adds an approximated area overhead of 5% for the column. It should be noted that modern memories are much bigger, so the area overhead significantly decreases for larger memories. Even more, read circuit in memory arrays may be shared for several columns.

Our proposal requires two additional control signals $I_{TEST,1}$ and $I_{TEST,2}$.

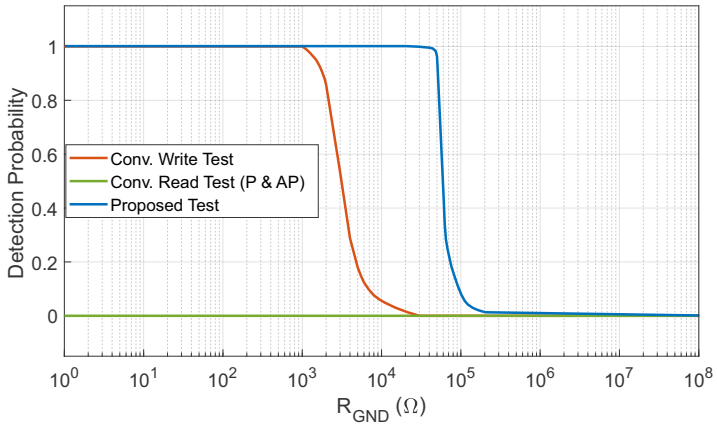


Fig. 18. Detection Probability for R_{GND} short.

7.3 Other Issues

Regarding test time, a logic test requires to perform multiple writes and reads operations. The test time of our proposal depends on the actual method to measure the currents (built-in or external). Our proposal does not add performance degradation because the transistors connected to BL and SL have the same sizes in the DFT read circuit and the original read circuit. Even more, our proposal presents robustness against process variations. The differential current amplifier cancels most of the variations in the memory, as they impact the current flowing into and out of the cell similarly.

7.4 Short Defects that Can Be Detected

The analysis above is based on assuming a defect modeling of short defects between supply rails (VDD and GND) and the internal node (nx) of the STT-MRAM cell. The proposed technique is valid to detect all those short defects that create an unbalanced current between BL and SL nodes. Note that resistive-open defects cannot be detected with the proposed approach, as these defects do not make different the current flowing through BL and SL terminals. Figure 19 shows a memory array, where some short defects that can be detected using the proposed approach are highlighted. The probability of occurrence of the short defects depends on the memory array architecture and how its layout is made. Typically, wider lines placed closer to other lines are more likely to present bridge defects [29]. The defects that are shown in Fig. 19 exhibit similar behavior to defects R_{VDD} and the R_{GND} in the defect model used in this work. Gate short defects between the W_{L0} and either B_{L0}, nx0, or S_{L0} behave as R_{VDD} because WL signal is settled to V_{DD} during a read operation to activate the access to the cell. Similarly, inter-cell shorts could be detected by previously setting the

voltages of the adjacent cell at adequate values. For example, $R_{BL0-SL1}$ behaves as R_{VDD} is S_{L1} terminal is set to V_{DD}. Therefore, the proposed test technique can cover a wide variety of manufacturing short defects.

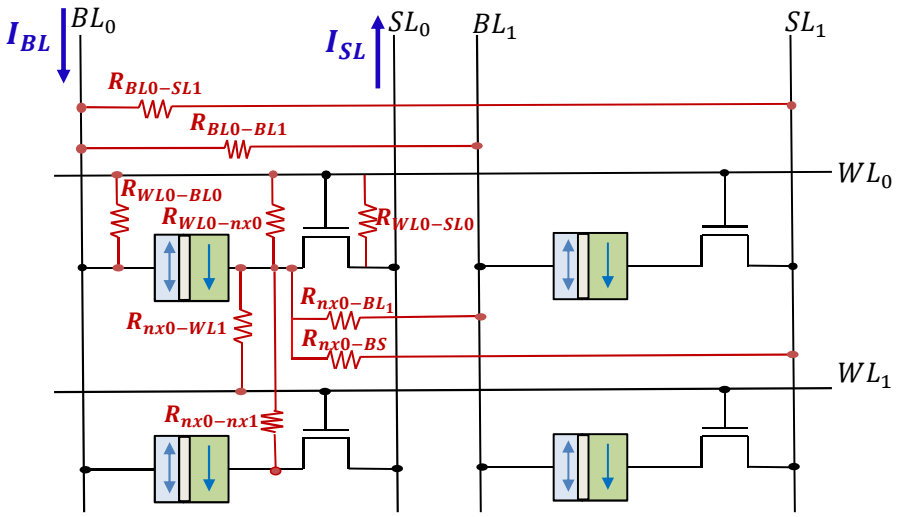


Fig. 19. Resistive shorts that can be detected using the proposed approach.

8 Conclusions

The behavior of an STT-MRAM cell under short defects in the presence of process variations has been analyzed. A DFT circuit for a defect-oriented test of resistive-shorts in an STT-MRAM cell was proposed. The proposed test technique is based on the observation that a short defect modifies the amplitude of the currents entering (I_{BL}) and leaving (I_{SL}) the memory cell. Thus, the DFT circuit senses the current difference between the currents I_{BL} and I_{SL}. The proposed approach is robust to process variations and significantly improves the detectability of resistive short defects that otherwise could escape to the conventional logic test. Detection probabilities of the resistive short defects are increased leading to high-quality electronic products.

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