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Reconfigurable Computing: Architectures, Tools and Applications

Third International Workshop, ARC 2007
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Preface

Reconfigurable computing platforms have been gaining wide acceptance, spanning a wide spectrum from highly specialized custom controllers to general-purpose high-end computing systems. They offer the promise of increasing performance gains by exploiting coarse-grain as well as fine-grain instruction level parallelism opportunities given their ability to implement custom functional, storage and interconnect structures. With the continuous increase in technology integration, leading to devices with millions of logic gates, ready to be programmed according to the (run-time) application needs, it is now possible to implement very sophisticated and reconfigurable systems. Configurability is seen as a key technology for substantial product life-cycle savings in the presence of evolving product requirements and/or interfaces or standards. The extreme configurability and flexibility also makes reconfigurable architectures the medium of choice for very rapid system prototyping or early design verification.

The relentless capacity growth of reconfigurable devices, such as FPGAs (Field-Programmable Gate Arrays), is creating a wealth of new opportunities and increasingly complex challenges. Recent generation devices have heterogeneous internal resources such as hardware multiplier units and memory blocks in addition to a vast amount of fine grain logic cells. Taking advantage of the wealth of resources in today's configurable devices is a very challenging problem. Although the inclusion of FPGAs in mainstream computing products clearly shows that this technology is maturing, many aspects still require substantial research to effectively deliver the promise of this emerging technology.

A major motivation for the International Applied Reconfigurable Computing (ARC)[1] workshop series is to provide a forum for presentation and discussion of on-going research efforts, as well as more elaborated, interesting and high-quality work, on applied reconfigurable computing. The workshop also focuses on compiler and mapping techniques, and new reconfigurable computing architectures.

The ARC series started in 2005 in the Algarve, Portugal. The second workshop (ARC 2006) took place in Delft, The Netherlands in March 2006, and the selected papers were published as a Springer LNCS (Lecture Notes in Computer Science) volume[2]. The success of previous workshops clearly reveals the growing interest of academia and industry and thus the timeliness of this forum.

This LNCS volume includes the papers selected for the third workshop (ARC 2007), held at Mangaratiba, Rio de Janeiro, Brazil, on March 27–29, 2007. The workshop attracted a large number of very good papers, describing interesting work on reconfigurable computing related subjects. A total of 72 papers

[1] http://www.arc-workshop.org

[2] Koen Bertels, João M. P. Cardoso, and Stamatis Vassiliadis (Eds.), Reconfigurable Computing: Architectures and Applications, Second International Workshop, ARC 2006, Delft, The Netherlands, March 2006, Revised Selected Papers, Springer Lecture Notes in Computer Science, LNCS 3985, August 2006.

were submitted to the workshop from 20 countries: The Netherlands (4), France (3), Germany (4), Republic of South Korea (12), Brazil (14), People's Republic of China (8), Denmark (1), Mexico (2), Portugal (2), South Africa (1), Lebanon (1), Australia (1), Republic of Ireland (2), Puerto Rico (1), Spain (5), UK (2), India (2), Japan (5), Poland (1), and Greece (1). Submitted papers were evaluated by at least three members of the Program Committee. After careful selection, 27 papers were accepted for presentation as full papers (37.5% of the total number of submitted papers) and 10 as short papers (global acceptance rate of 51.4%). This volume also includes an article from the 2006 ARC workshop, which was, by lapse, not included in the 2006 proceedings. Those accepted papers led to a very interesting workshop program, which we considered to constitute a representative overview of ongoing research efforts in reconfigurable computing, a rapidly evolving and maturing field.

Several persons contributed to the success of the workshop. We would like to acknowledge the support of all the members of this year's workshop Steering and Program Committees in reviewing papers, in helping with the paper selection, and in giving valuable suggestions. Special thanks also to the additional researchers who contributed to the reviewing process, to all the authors who submitted papers to the workshop, and to all the workshop attendees. We also acknowledge the generous financial contribution from Altera Corp., USA and PI Componentes, Brazil. Last but not least, we are especially indebted to our colleague Jürgen Becker from the University of Karlsruhe for his strong support of this workshop.

We are grateful to Springer, particularly Mr. Alfred Hofmann and the LNCS Editorial, for their support and work in publishing this book.

January 2007

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The 2007 Applied Reconfigurable Computing workshop (ARC 2007) was organized by the Institute of Mathematics and Computer Science (ICMC) of the University of São Paulo (USP) in São Carlos, Brazil.

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