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Integrated Circuit and System Design

Power and Timing Modeling, Optimization and Simulation

20th International Workshop, PATMOS 2010
Grenoble, France, September 7-10, 2010
Revised Selected Papers

Springer

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Preface

Welcome to the proceedings of the 20th International Workshop on Power and Timing Modeling, Optimization and Simulations, PATMOS 2010. Over the years, PATMOS has evolved into an important European event, where researchers from both industry and academia discuss and investigate the emerging challenges in future and contemporary applications, design methodologies, and tools required for the development of the upcoming generations of integrated circuits and systems. PATMOS 2010 was organized by the TIMA Laboratory, France, with the sponsorship of Joseph Fourier University, CEA LETI, Minalogic, CNRS, Grenoble Institute of Technology and the technical co-sponsorship of the IEEE France Section. Further information about the workshop is available at: http://patmos2010.imag.fr.

The technical program of PATMOS 2010 contained state-of-the-art technical contributions, three invited keynotes, a special session organized by the "Beyond DREAMS (Catrene 2A717)" project on "High-Level Modeling of Power-Aware Heterogeneous Designs in SystemC-AMS" and a special session organized by Minalogic presenting the results of four projects.

The technical program focused on timing, performance, and power consumption, as well as architectural aspects with particular emphasis on modeling, design, characterization, analysis, and optimization in the nanometer era.

The Technical Program Committee, with the assistance of additional expert reviewers, selected the 24 papers presented at PATMOS. The papers were organized into six oral sessions. As is customary for the PATMOS workshops, full papers were required for review, and a minimum of three reviewers were received per manuscript.

Beyond the presentations of the papers, the PATMOS technical program was enriched by a series of talks offered by world-class experts, on important emerging research issues of industrial relevance. Kiyoo Itoh Fellow of Central Research Laboratory, Hitachi, Ltd., spoke about "Variability-Conscious Circuit Designs for Low-Voltage Memory-Rich Nano-Scale CMOS LSIs," Marc Belleville of CEA, LETI, MINATEC, spoke about "3D Integration for Digital and Imagers Circuits: Opportunities and Challenges," and Sébastien Marchal of STMicroelectonics spoke about "Signing off Industrial Designs on Evolving Technologies."

We would like to thank our colleagues who voluntarily worked to make this edition of PATMOS possible: the expert reviewers; the members of the Technical Program and Steering Committees; the invited speakers; and last but not least, the local personnel who offered their skill, time, and extensive knowledge to make PATMOS 2010 a memorable event.

September 2010

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Gilles Sicard

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