

Editor-in-Chief

*A. Joe Turner, Seneca, SC, USA*

Editorial Board

Foundations of Computer Science

*Mike Hinchey, Lero, Limerick, Ireland*

Software: Theory and Practice

*Michael Goedicke, University of Duisburg-Essen, Germany*

Education

*Arthur Tatnall, Victoria University, Melbourne, Australia*

Information Technology Applications

*Ronald Waxman, EDA Standards Consulting, Beachwood, OH, USA*

Communication Systems

*Guy Leduc, Université de Liège, Belgium*

System Modeling and Optimization

*Jacques Henry, Université de Bordeaux, France*

Information Systems

*Jan Pries-Heje, Roskilde University, Denmark*

ICT and Society

*Jackie Phahlamohlaka, CSIR, Pretoria, South Africa*

Computer Systems Technology

*Paolo Prinetto, Politecnico di Torino, Italy*

Security and Privacy Protection in Information Processing Systems

*Kai Rannenberg, Goethe University Frankfurt, Germany*

Artificial Intelligence

*Tharam Dillon, Curtin University, Bentley, Australia*

Human-Computer Interaction

*Annelise Mark Pejtersen, Center of Cognitive Systems Engineering, Denmark*

Entertainment Computing

*Ryohei Nakatsu, National University of Singapore*

## **IFIP – The International Federation for Information Processing**

IFIP was founded in 1960 under the auspices of UNESCO, following the First World Computer Congress held in Paris the previous year. An umbrella organization for societies working in information processing, IFIP's aim is two-fold: to support information processing within its member countries and to encourage technology transfer to developing nations. As its mission statement clearly states,

*IFIP's mission is to be the leading, truly international, apolitical organization which encourages and assists in the development, exploitation and application of information technology for the benefit of all people.*

IFIP is a non-profitmaking organization, run almost solely by 2500 volunteers. It operates through a number of technical committees, which organize events and publications. IFIP's events range from an international congress to local seminars, but the most important are:

- The IFIP World Computer Congress, held every second year;
- Open conferences;
- Working conferences.

The flagship event is the IFIP World Computer Congress, at which both invited and contributed papers are presented. Contributed papers are rigorously refereed and the rejection rate is high.

As with the Congress, participation in the open conferences is open to all and papers may be invited or submitted. Again, submitted papers are stringently refereed.

The working conferences are structured differently. They are usually run by a working group and attendance is small and by invitation only. Their purpose is to create an atmosphere conducive to innovation and development. Refereeing is less rigorous and papers are subjected to extensive group discussion.

Publications arising from IFIP events vary. The papers presented at the IFIP World Computer Congress and at open conferences are published as conference proceedings, while the results of the working conferences are often published as collections of selected and edited papers.

Any national society whose primary activity is in information may apply to become a full member of IFIP, although full membership is restricted to one society per country. Full members are entitled to vote at the annual General Assembly. National societies preferring a less committed involvement may apply for associate or corresponding membership. Associate members enjoy the same benefits as full members, but without voting rights. Corresponding members are not represented in IFIP bodies. Affiliated membership is open to non-national societies, and individual and honorary membership schemes are also offered.

José L. Ayala David Atienza Alonso  
Ricardo Reis (Eds.)

# VLSI-SoC: Forward-Looking Trends in IC and Systems Design

18th IFIP WG 10.5/IEEE International Conference  
on Very Large Scale Integration, VLSI-SoC 2010  
Madrid, Spain, September 27-29, 2010  
Revised Selected Papers

Volume Editors

José L. Ayala  
Complutense University of Madrid, Computer Science Faculty  
28040 Madrid, Spain  
E-mail: jayala@fdi.ucm.es

David Atienza Alonso  
École Polytechnique Fédérale de Lausanne (EPFL)  
Institute of EE, Embedded Systems Laboratory  
ELG 131, Station 11, 1015 Lausanne, Switzerland  
E-mail: david.atienza@epfl.ch

Ricardo Reis  
Universidade Federal do Rio Grande do Sul, Instituto de Informática  
Av. Bento Gonçalves, 9500, Campus do Vale  
Bloco IV, CP 15064, 91501-970 Porto Alegre, Brazil  
E-mail: reis@inf.ufrgs.br

ISSN 1868-4238  
ISBN 978-3-642-28565-3  
DOI 10.1007/978-3-642-28566-0  
Springer Heidelberg Dordrecht London New York

e-ISSN 1868-422X  
e-ISBN 978-3-642-28566-0

Library of Congress Control Number: 2012931869

CR Subject Classification (1998): B.7-8, C.0, F.2, J.2-3, C.2.1

© IFIP International Federation for Information Processing 2012

This work is subject to copyright. All rights are reserved, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, re-use of illustrations, recitation, broadcasting, reproduction on microfilms or in any other way, and storage in data banks. Duplication of this publication or parts thereof is permitted only under the provisions of the German Copyright Law of September 9, 1965, in its current version, and permission for use must always be obtained from Springer. Violations are liable to prosecution under the German Copyright Law.

The use of general descriptive names, registered names, trademarks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

*Typesetting:* Camera-ready by author, data conversion by Scientific Publishing Services, Chennai, India

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

# Preface

This book contains extended and revised versions of the best papers that were presented during the 18th edition of the IFIP/IEEE WG10.5 International Conference on Very Large Scale Integration, a global System-on-a-Chip Design and CAD conference. The 18th conference was held at the Complutense University, Madrid, Spain (September 27–29, 2010). Previous conferences have taken place in Edinburgh, Trondheim, Vancouver, Munich, Grenoble, Tokyo, Gramado, Lisbon, Montpellier, Darmstadt, Perth, Nice, Atlanta, Rhodes and Florianópolis.

The purpose of this conference sponsored by IFIP TC 10 Working Group 10.5, the IEEE Council on Electronic Design Automation (CEDA), and by IEEE Circuits and Systems Society, with the In-Cooperation of ACM SIGDA, is to provide a forum to exchange ideas and show industrial and academic research results in the field of microelectronics design. The current trend toward increasing chip integration and technology process advancements brings about stimulating new challenges both at the physical and system-design levels, as well in the test of these systems. VLSI-SOC conferences aim to address these exciting new issues.

The 2010 edition of VLSI-SoC maintained the traditional structure, which has been successful at the previous VLSI-SOC conferences. The quality of submissions (175 papers from 22 countries) made the selection process difficult, but finally 52 papers for oral presentation and 17 posters were accepted for presentation in VLSI-SoC 2010. Out of the 52 full papers presented at the conference, 14 regular papers were chosen by a selection committee to have an extended and revised version included in this book. The chapters of this book have authors from Belgium, China, Egypt, France, Singapore, Spain, Switzerland, Taiwan and the USA. The Technical Program Committee was composed of 109 members.

VLSI-SoC 2010 was the culmination of many dedicated volunteers: paper authors, reviewers, session chairs, invited speakers and various committee chairs, especially the local arrangements organizers. We thank them all for their contribution.

This book is intended for the VLSI community, mainly those who did not have the chance to take part in the VLSI-SOC 2010 conference. The papers were selected to cover a wide variety of excellence in VLSI technology and the advanced research they describe. We hope you will enjoy reading this book and find it useful in your professional life and for the development of the VLSI community as a whole.

December 2011

José L. Ayala  
David Atienza  
Ricardo Reis



## **PhD Forum Chairs**

Matthew Guthaus

UCSC, USA

Andreas Burg

ETHZ, Switzerland

## **Institutional Relations Chairs**

Roman Hermida

Complutense University, Spain

Francisco Tirado

Complutense University, Spain

## **Steering Committee**

Manfred Glesner

TU Darmstadt, Germany

Salvador Mir

TIMA, France

Ricardo Reis

UFRGS, Brazil

Michel Robert

LIRMM, France

Luis Miguel Silveira

INESC ID, Portugal

# Table of Contents

A 1-V CMOS Ultralow-Power Receiver Front End for the IEEE 802.15.4 Standard Using Tuned Passive Mixer Output Pole . . . . .	1
<i>Aaron V.T. Do, Chirn Chye Boon, Manthena Vamshi Krishna, Anh Manh Do, and Kiat Seng Yeo</i>	
Self-Timed Rings: A Promising Solution for Generating High-Speed High-Resolution Low-Phase Noise Clocks . . . . .	22
<i>Oussama Elissati, Sébastien Rieubon, Eslam Yahya, and Laurent Fesquet</i>	
Adaptive Logical Control of RF LNA Performances for Efficient Energy Consumption . . . . .	43
<i>Rafik Khereddine, Louay Abdallah, Emmanuel Simeu, Salvador Mir, and Fabio Cenni</i>	
A 1.8-V 3.6-mW 2.4-GHz Fully Integrated CMOS Frequency Synthesizer for the IEEE 802.15.4 . . . . .	69
<i>Manthena Vamshi Krishna, Xuan Jie, Anh Manh Do, Chirn Chye Boon, Kiat Seng Yeo, and Aaron V.T. Do</i>	
Design and Optimization of a Digital Baseband Receiver ASIC for GSM/EDGE . . . . .	100
<i>Christian Benkeser and Qiuting Huang</i>	
VLSI Implementation of Hard- and Soft-Output Sphere Decoding for Wide-Band MIMO Systems . . . . .	128
<i>Christoph Studer, Markus Wenk, and Andreas Burg</i>	
Joint Optimization of Low-Power DCT Architecture and Efficient Quantization Technique for Embedded Image Compression . . . . .	155
<i>Maher Jridi and Ayman Alfalou</i>	
Fast Fixed-Point Optimization of DSP Algorithms . . . . .	182
<i>Gabriel Caffarena, Ángel Fernández-Herrero, Juan A. López, and Carlos Carreras</i>	
Design and Verification of Lazy and Hybrid Implementations of the SELF Protocol . . . . .	206
<i>Eliyah Kilada and Kenneth S. Stevens</i>	
Adaptation Strategies in Multiprocessors System on Chip . . . . .	233
<i>Remi Busseuil, Gabriel Marchesan Almeida, Luciano Ost, Sameer Varyani, Gilles Sassatelli, and Michel Robert</i>	

Tri-mode Operation for Noise Reduction and Data Preservation in  
Low-Leakage Multi-Threshold CMOS Circuits ..... 258  
*Hailong Jiao and Volkan Kursun*

Fast Legalization for Standard Cell Placement with Simultaneous  
Wirelength and Displacement Minimization ..... 291  
*Tsung-Yi Ho and Sheng-Hung Liu*

Control Electronics Integration toward Endoscopic Capsule Robot  
Performing Legged Locomotion and Illumination ..... 312  
*Oscar Alonso and Angel Diéguez*

Smart Camera System-on-Chip Architecture for Real-Time Brush  
Based Interactive Painting Systems ..... 339  
*Luc Claesen, Peter Vandoren, Tom Van Laerhoven, Andy Motten,  
Fabian Di Fiore, Frank Van Reeth, Jing Liao, and Jinhui Yu*

**Author Index** ..... 355