Lecture Notes in Computer Science 7165

Commenced Publication in 1973
Founding and Former Series Editors:
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Reversible Computation

Third International Workshop, RC 2011
Gent, Belgium, July 4-5, 2011
Revised Papers

Springer

Volume Editors

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ISSN 0302-9743 e-ISSN 1611-3349
ISBN 978-3-642-29516-4 e-ISBN 978-3-642-29517-1
DOI 10.1007/978-3-642-29517-1
Springer Heidelberg Dordrecht London New York

Library of Congress Control Number: 2012935141

CR Subject Classification (1998): F.3, D.2, D.3, F.2, C.2, F.1

LNCS Sublibrary: SL 2 – Programming and Software Engineering

Typesetting: Camera-ready by author, data conversion by Scientific Publishing Services, Chennai, India

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

Preface

In recent years, reversible computation has established itself as a very promising research area and an emerging technology. This is motivated by a widely supported prediction that the conventional computer hardware technologies are going to reach their limits in the not-too-distant future.

In particular, the impact of power consumption of electronic devices on the intended behavior of such devices is becoming a serious problem. While the unwanted behavior of transistors can be reduced by higher levels of integration and new fabrication processes, a more fundamental problem exists: As proven by Landauer in 1961, each time a bit of information is deleted exactly $k \cdot T \cdot \log 2$ Joule of energy is dissipated, where k is the Boltzmann constant and T is the temperature. While this amount of energy does not seem presently significant, it forms potentially a barrier for future technologies. Transistors that perform millions of operations per second are fairly common these days, and more and more operations are performed on smaller and smaller transistors. Since these trends are most likely to continue, dissipation of $k \cdot T \cdot \log 2$ Joule of energy per bit of information lost will become crucial and may bring the progress of conventional computer technologies to a halt.

In contrast, reversible computations may reduce or even eliminate this power dissipation. This holds since n-input n-output functions, for some appropriate n, can be used to map each possible input vector to a unique output vector. Data are bijectively transformed in this way without losing any of the original information, thus avoiding energy dissipation. In fact, computations with zero power dissipation are only possible provided they are performed in a reversible manner. Thus, in order to overcome the limitations caused by Landauer's barrier, computation has to be reversible.

Moreover, quantum computation has become a major application area for reversible logic. It uses qubits instead of the conventional bits. Qubits allow one to represent not only 0 and 1 but also a superposition of both. As a result, qubits can represent multiple states at the same time theoretically enabling enormous speed-ups in computation. It has been shown that, for example, using a quantum circuit it is possible to solve the factorization problem in polynomial time while for conventional circuits only exponential methods exist. Admittedly, although the research in the domain of quantum circuits is still in its infancy, the first simple quantum circuits are being physically implemented. Reversible computation is therefore essential because every quantum operation is inherently reversible. Thus, progress in the domain of reversible logic can be directly applied to quantum logic.

Further applications of reversible computation paradigms can be found in coding/decoding, program debugging, testing, database recovery, discrete event simulation, reversible algorithms, reversible specification formalisms, reversible

programming languages, process algebras and semantics of concurrency, or the modeling of biochemical systems.

The Workshop on Reversible Computation provides a platform to present and to discuss new trends and recent developments in this promising area. Previous events took place in March 2009 in York, UK (with proceedings published as ENTCS Volume 253, Issue 6) and in July 2010 in Bremen, Germany (with proceedings published in the *Journal of Multiple-Valued Logic and Soft Computing* Volume 18, Issue 1).

The volume at hand covers revised and extended versions of the best papers presented at the third edition of the Workshop on Reversible Computation which took place in Gent, Belgium, during July 4–5, 2011. From a total of 25 original submissions, the Program Committee selected 10 submissions for publication in this issue (leading to an acceptance rate of 40%). For this purpose, an intensive double-blind review process was conducted.

The first paper considers a theoretical aspect of reversible computation. The author H.B. Axelsen studies the time complexity of tape reduction in reversible Turing machines. While it was already known that the reduction from k tapes to 1 tape in general leads to a quadratic increase in time, for k to 2 tapes a reduction to a logarithmic factor is possible.

Ways toward a functional language for reversible computations are described in the second paper. T. Yokoyama, H.B. Axelsen, and R. Glück identify the basic concepts such a language has to satisfy and discuss the advantages using several example programs.

Logic design is considered in the following three papers. M.K. Thomsen, H.B. Axelsen, and R. Glück describe the design of a purely reversible processor architecture and its instruction set. Therefore, a simple, yet expressive, locally invertible instruction set, and fully reversible control logic and address calculation, is applied. Optimization techniques for reversible circuits based on templates are introduced by M.M. Rahman, G.W. Dueck, and A. Banerjee, who make use of a newly developed splitting rule. Finally, C. Moraga presents an extension of the commonly used Toffoli gates enabling one to efficiently realize operations in GF(2) and lattice operations of a Boolean algebra.

The sixth paper presents a software toolkit called RevKit that assists users in the design of reversible circuits. RevKit is developed by M. Soeken, S. Frehse, R. Wille, and R. Drechsler. It provides various functionalities ranging from synthesis and optimization to verification of reversible circuits. Furthermore, RevKit is open source so that other researchers can use and extend its functionalities.

The application of reversible computation to the domain of quantum circuits is covered in the seventh and eighth paper. Z. Sasanian and D.M. Miller propose a mapping of reversible gate into quantum gates using the NCVW library instead of the previously applied NCV library. Afterwards, quantum circuit synthesis considering linear nearest neighbor architectures is considered by A. Matsuo and S. Yamashita.

Finally, physical realizations of reversible circuits in CMOS technologies is the subject of the last two papers. First, S. Burignat, M. Olczak, M. Klimczak, and

A. De Vos discuss key questions rising from existing reversible dual-line pass-transistor technology. Afterwards, a technical solution that allows interfacing reversible pass-transistor logic with conventional CMOS logic is presented by S. Burignat, M.K. Thomsen, M. Klimczak, M. Olczak, and A. De Vos.

We would like to thank all the authors for their valuable contributions to this special issue devoted to RC 2011. Furthermore, many thanks are due to the members of the Program Committee and all external reviewers for their excellent work in evaluating the submissions as well as for providing detailed feedback and further suggestions to the authors. Finally, we wish to thank Alfred Hofmann of Springer for agreeing to publish these proceedings in the book series Springer *Lecture Notes in Computer Science*. Support from the University of Ghent and the University of Bremen is also gratefully acknowledged.

November 2011

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