Journal of Electronic Testing (2020) 36:143–144
https://doi.org/10.1007/s10836-020-05876-3

Editorial

Vishwani D. Agrawal[1]

Received: 29 March 2020 / Accepted: 29 March 2020 / Published online: 22 April 2020

This issue contains ten articles. The topics discussed are hardware security, mixed-signal testing, RF testing, microfluidic biochip testing, verification, 3D stacked device testing, memory testing and test generation.

In October 2019, we published a special issue of articles from a joint conference, the 32*nd International Conference on VLSI Design* and 18*th International Conference on Embedded Systems* that took place in New Delhi, India during January 5–9, 2019. Our guest editors invited a set of highest rated conference papers. Ten of those papers appeared in October 2019, but one was late and is appearing as the first paper of this issue. Guest Editor Kanad Basu was responsible for its processing.

Three other papers in this issue have come from two separate conferences. The third article is an expanded version of a paper from the *Twenty-eighth IEEE North Atlantic Test Workshop* (NATW), Essex, Vermont, held during May 13–15, 2019. Professor Themistoklis Haniotakis served as Guest Editor for it. Papers appearing as fourth and ninth are expanded versions of those appearing at the *Twentieth IEEE Latin-American Test Symposium* (LATS), held during March 11–13, 2019 in Santiago, Chile. *JETTA* Editors Leticia M. B. Poehls and Patrick Girard are responsible for peer reviewing of the journal versions of the two papers, respectively.

The first paper in this issue addresses hardware security. Authors are Srivastava from Qualcomm, Bengaluru, India and Ghosh from NXP Semiconductors, India Design Center. In their proposal, once a security violation occurs, built-in self-test (BIST) hardware already present in the memory erases the sensitive data.

The second paper gives a technique to estimate the remaining useful life (RUL) of an analog circuit. First, an analysis determines the time dependent degradation rates for circuit components. That information then allows determination of the time to expected failure of the circuit. The authors are Rathnapriya and Manikandan from Coimbatore Institute of Technology, Coimbatore, India.

Next, two papers focus on radio frequency (RF) test.

The third paper develops a method for measuring dielectric properties, such as dielectric constant and loss tangent, of thin films used in RF components. This technique uses a coplanar waveguide test structure. Contributors are Ge and Wang from University of South Carolina, Columbia, SC, USA and Xia from University of Vermont, Burlington, VT, USA.

In the fourth paper, El Badawi, Azais, Bernard, Comte and Kerzerho from LIRMM, University of Montpellier, CNRS, Montpellier Cedex, France and Lefevre from NXP Semiconductors, Caen, France revisit alternate or indirect test methodology. They use machine learning to improve the accuracy of the test result by combining multiple indirect measurements.

The fifth paper is on testing of microfluidic chips and authors are Huang, Xu and Zhang from Guilin University of Electronic Technology, Guilin, China. Their test has a single droplet traversing a minimal path that covers all fluid links in the device. The paper discusses both on-line and off-line tests.

The sixth paper addresses the verification issue. Authors are Sharma and Bhargava from Malaviya National Institute of Technology, Jaipur, Rajasthan, India and Kumar from NXP Semiconductors, Noida, Uttar Pradesh, India. The main idea in this work is to improve the, so-called, universal verification methodology (UVM) in which a typical testbench may consist of random test cases. Basic improvements come from automation in test case generation, which aims at improving the functional coverage.

The seventh paper related to testability of 3D stacked devices proposes a method to minimize the test wrapper length. The authors use particle swarm optimization (PSO) based metaheuristic approach for placement of wrapper chains, requiring a minimal number of through silicon vias (TSV). Contributors of this paper are Kaibartta and Biswas from Indian Institute of Technology (Indian School of Mines), Dhanbad, India and Das from Jadavpur University, Kolkata, India.

✉ Vishwani D. Agrawal
agrawvd@auburn.edu

[1] Auburn University, Auburn, AL 36849, USA

Memory testing is the topic of the next two papers.

The eighth paper proposes a 10-transistor radiation hardened memory cell. This cell has a read decoupled path to improve read static noise margin (RSNM) and contains a voltage booster between storage nodes to increase capacitance. Authors are Shah from Technische Universität at Wien, Vienna, Austria, Vishvakarma from Indian Institute of Technology, Indore, MP, India and Hübner from Brandenburg University of Technology, Cottbus, Germany.

The ninth paper investigates the behavior of a memory cell with resistive defects, when operating under various power supply voltages, using SPICE simulation. FinFET based cell shows greater sensitivity to the defect compared to the CMOS based cell. In addition, temperature rise further increases the defect sensitivity of the FinFET cell. Authors are Copetti and Balen from Federal University of Rio Grande do Sul – UFRGS, Porto Alegre, Brazil, and Brum, Aquistapace and Bolzani Poehls from Pontifical Catholic University of Rio Grande do Sul – PUCRS, Porto Alegre, Brazil.

In the tenth paper, Fooladi and Kamran from Razi University, Kermanshah, Iran propose the use of probabilistic methods, instead of the traditional fault simulation, in automatic test pattern generation (ATPG). They develop a probabilistic analysis of the circuit structure using four-valued signals. Similar to fault simulation, this analysis considers many faults simultaneously to estimate coverage by a given input pattern. The probabilistic analysis is faster than fault simulation by at least two orders of magnitude.