Analysis of Dampers in Time-Sensitive Networks with Non-ideal Clocks

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***Abstract*—Dampers are devices that reduce delay jitter in the context of time-sensitive networks, by delaying packets for the amount written in packet headers. Jitter reduction is required by some real-time applications; beyond this, dampers have the potential to solve the burstiness cascade problem of deterministic networks in a scalable way, as they can be stateless. Dampers exist in several variants: some apply only to earliest-deadline-first schedulers, whereas others can be associated with any packet schedulers; some enforce FIFO ordering whereas some others do not. Existing analyses of dampers are specific to some implementations and some network configurations; also, they assume ideal, non-realistic clocks. In this paper, we provide a taxonomy of all existing dampers in general network settings and analyze their timing properties in presence of non-ideal clocks. In particular, we give formulas for computing residual jitter bounds of networks with dampers of any kind. We show that non-FIFO dampers may cause reordering due to clock non-idealities and that the combination of FIFO dampers with non-FIFO network elements may very negatively affect the performance bounds. Our results can be used to analyze timing properties and burstiness increase in any time-sensitive network, as we illustrate on an industrial case-study.**

I. Introduction

Time-sensitive networks provide guarantees for applications in the automobile, automation, space, avionics and video industries [1]–[6]. IEEE Time Sensitive Networking (TSN) working group [7] and the IETF Deterministic Networking (DetNet) working group [8] provide standardization for such networks. The goal of time-sensitive networks is to fulfill flow requirements on worst-case delay and jitter (defined as the difference between worst-case and best-case delays), in-order packet delivery, as well as zero congestion loss and seamless redundancy [9], [10]. The emergeance of applications with low jitter requirement in large-scale time-sensitive networks, such as industrial Internet of Things [11] and electricity distribution [12], questions the performance of existing queuing and shaping mechanisms such as Credit-Based Shaper, IEEE 802.1Qch Cyclic Queuing and Forwarding (CQF) [13], and Deficit Round Robin [14]. This issue can be addressed with dampers, which are mechanisms to reduce delay jitter in time-sensitive networks [15]–[17].

A damper delays every time-sensitive packet by an amount written in a packet header field, called damper header, which carries an estimate of the earliness of this packet with respect to a known delay upper-bound of upstream systems. This ideally leads to zero jitter; in practice, there is still some small residual jitter, due to errors in acquiring timestamps and in computing and implementing delays. As a positive side effect, dampers create packet timings that are almost the same as at the source, with small errors due to residual jitter, and thus cancel most of the burstiness increase imposed by the network. [18, Lemma 1]. The residual burstiness increase that remains when dampers are used is not influenced by the burstiness of cross-traffic. Thus, dampers solve the burstiness cascade issue [19]: individual flows that share a resource dedicated to a class may see their burstiness increase, which may in turn increase the burstiness of other downstream flows. Furthermore, dampers are stateless, unlike some TSN shaping mechanisms, e.g., Asynchronous Traffic Shaping (ATS) [20]. Solving the burstiness cascade in a stateless manner makes the dampers of interest for large-scale time-sensitive networks.

Several implementations of dampers have been proposed; the older ones are associated with specific schedulers such as earliest-deadline-first [15], [17] and static priority [16]; the recent implementations can coexist with any scheduling mechanism [21]–[23]. Some of these implementations enforce dampers to behave in a FIFO manner [17], [21], [23] and some do not [16], [22]. Analysis of damper is crucial to provide guarantees for applications in the context of time-sensitive networks. In the existing works, [22], [23] did not provide any analysis; others analyze only their implementation and under limited assumptions on the network settings. Also, existing analyses assume that the network operates with one ideal clock; in practice, this assumption does not hold and may have non-negligible side effects. Recently, the effect of non-ideal clocks on regulators was analyzed and a clock model was proposed in the context of time-sensitive networks [24], which we use in this paper.

We first present a taxonomy of dampers that classifies the existing implementations into dampers with or without FIFO constraint. Then, under general network configuration with non-ideal clocks, we provide formulas to compute tight delay and jitter bounds for dampers without FIFO constraint (Theorems 1 and 2); we see that the impact of non-ideal clocks can be non-negligible in cases with low jitter requirements. As a result of this analysis, we derive conditions in which clock synchronization throughout a network does not affect the performance of dampers. Moreover, we capture the propagation of arrival curve at the output of dampers and see how this can solve the burstiness cascade issue. Next, we show that existing

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implementations of dampers without FIFO constraints may cause undesired packet reordering due to clock non-idealities, even in synchronized networks. This problem is avoided with dampers that enforce FIFO constraints; however, the effect on their timing properties was not analysed in the literature and we bridge this gap in this paper. We model two classes of dampers with FIFO constraint: re-sequencing dampers and head-of-line dampers. For the former class, we show that when all network elements are FIFO, the delay and jitter bounds are not affected by the re-sequencing operation (Theorem 3). For the latter class, there is a small penalty due to head-of-line queuing, which we quantify exactly (Theorem 4). In contrast, if some network elements are non FIFO, the jitter bounds for dampers with FIFO constraint can be considerably larger (Theorems 5 and 6). We finally evaluate our results in an industrial case-study.

The rest of the paper is as follows. Section II presents the state-of-the-art. Section III describes the system model, terminology, clock model and all assumptions. Section IV presents a taxonomy of the existing dampers. The analysis of dampers without FIFO constraint is presented in Section V. Packet reordering scenarios due to non-ideal clocks are presented in Section VI. The analysis of dampers with FIFO constraint is given in Section VII. Section VIII provides a numerical evaluation for an industrial case-study and Section IX concludes the paper.

II. Related Works

The concept of dampers was introduced by Verma et. al [15], under the name *delay-jitter regulator*, in combination with earliest-deadline-first (EDF) scheduling. In this scheme, a per-flow regulator is placed at every node to delay a packet as much as its earliness in the previous node; the earliness is the time difference between the delay that a packet was supposed to experience and the actual delay that is measured by time-stamping. Later, Zhang et. al. [16] proposed Rate-Control Static Priority (RCSP) scheduling to avoid coupling of delay and bandwidth allocation in the EDF schedulers mentioned in [15]. We describe RCSP in Section IV.

The term *damper* was first used by Rene Cruz [17] as a conceptual network element that slows down the traffic passing through it. In [17], dampers are used in relationship with SCED (Service Curve Earliest Deadline) scheduling to avoid extra queuing as was proposed by [16]. With this scheme, called SCED+, a flow traverses a few virtual paths (each is a sequence of switches) with guaranteed service curves and damper curves. Then, at the entrance of each virtual path, for every packet of the flow and every switch in the virtual path, initial and terminal eligibility times are computed using the service and damper curves; a packet is released from a switch within its initial and terminal eligibility times.

Recently, a few implementations of damper are proposed that can be used in combination with any scheduling mechanism. Grigorjew et. al. [21] implement damper as a shaper in relation with Asynchronous Traffic Shaping (ATS), IEEE 802.1 Qcr [20]; we refer to their scheme as jitter-control ATS. It is assumed in [21] that the input flows are constrained by leaky-bucket arrival curve and all the elements inside the network, including the switching fabrics, output port queues and the ATS, are FIFO for the packets that share the same queues inside ATS. Rotated gate-control-queues (RGCQ) [22] is an implementation of a damper integrated with the queuing system of a scheduler. Flow-order preserving latency-equalizer (FOPLEQ) [23] is as an extension of RGCQ to preserve the per-flow order of the packets according to its entrance to FOPLEQ. Section IV describes the details of these implementations. These previous works do not provide delay analysis or do it in restricted settings. In particular, clock non-idealities are ignored. In [24] clock non-idealities are modelled in the context of time-sensitive networks and the impact on timing analyses is explained in detail. In this paper, we apply this clock model to networks with dampers of various kinds.

Dampers can be used to reduce delay jitter and thus to provide end-to-end services with a low jitter guarantee. An alternative method to provide low jitter, Cyclic Queuing and Forwarding (CQF), also known as Peristaltic Shaper, was introduced by IEEE Time-Sensitive Networking (TSN) [13], [25, Annex T]. According to CQF, for each priority class, there are two cyclic queues; in each cycle, while one queue is being served, the other enqueues the arriving packets. The cycles change periodically and the queues swap their operations with each other. CQF relies on very different mechanisms and assumptions than dampers; its analysis is out of the scope of this paper.

III. System Model

We consider a network that contains a set switches or routers, hosts and links with fixed capacity. Every flow follows a fixed path, has a finite lifetime and emits a finite, but arbitrary, number of packets. We consider unicast flows with known arrival curves at their sources (i.e. there are known bounds on the number of bits or packets that can be emitted by a flow within any period of time).

A. Terminology

We call *jitter-compensated system* (JCS) any delay element or aggregate of delay elements with known delay and jitter bounds, for which we want to compensate jitter by means of dampers. This is typically the queuing system on the output port of a switch or router used in time-sensitive networks. It can also be a switching fabric or an input port processing unit, or even a larger system. For time-sensitive flows, a JCS should be able to time stamp packet arrivals and departures using the available local times. It should also increment the damper header field in every time-sensitive packet (if one is present) by an amount equal to an estimate of the earliness of this packet with respect to the known delay upper-bound at the JCS for the class of traffic that this packet belongs to. If no damper header is present, it inserts one, with a value equal to the estimated earliness.[1] The operation of the damper

[1]We choose this method of carrying earliness in packet headers for ease of presentation. Another method consists in each JCS inserting a separate damper header: a packet then has as many damper headers as JCSs between dampers, and the earliness to be compensated at a damper is the sum of all these values. The discussion of such methods is out of the scope of this paper, as it does not affect the timing analysis presented here.

header update (DHU) unit is described in Section IV-C. When a time-sensitive flow crosses a JCS, for actual jitter removal to occur, there must be a downstream damper on the path of the flow. For example, if the JCS is a switch output port, the next downstream damper is typically located on the output port of the next downstream switch.

It is generally not possible, or required, to remove delay jitter in all network elements, because time stamping and DHU come with a cost. Therefore, it is required, for our timing analysis, to consider what we call *bounded-delay systems* (BDSs), defined as any delay element or aggregate of delay elements with known delay and jitter bounds, and for which we do not compensate jitter. Constant delay elements (e.g. an output link propagation delay), variable delay elements with very low jitter (e.g., very high speed backbone network) and other delay elements without DHU unit are examples of BDSs.

A *damper* is a system that delays every time-sensitive packet, using its local clock, for a duration approximately equal to the damper header (if any, else the damper does not delay the packet). Such a damper header was inserted/updated in the upstream JCSs between this damper and the previous upstream damper or the source of the flow. The damper also resets the damper header, so that the next downstream damper will see only the earliness accumulated downstream of this damper. Designing a stand-alone damper is a challenge, because such a damper may need to release a large number of packets instantly or within a very short time, which might not be feasible. This is why damper implementations are often associated with queuing systems; then, the time at which a damper releases a packet is simply the time at which the packet becomes visible to the queuing system. We classify and model existing designs of dampers in Section IV.

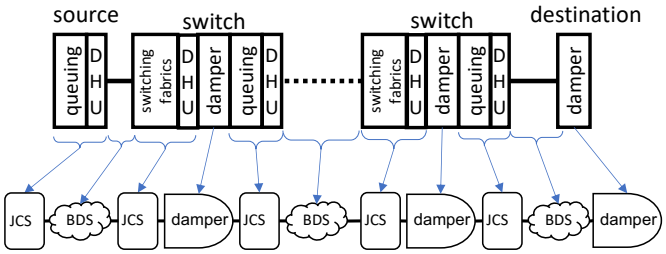

Fig. 1: A local-area time-sensitive network example.

Example 1. Fig. 1 shows an example flow path within a local-area time-sensitive network where we want to compensate the jitter imposed by the output queuing systems and switching fabrics by means of dampers. Therefore, for each of the switching fabrics and the queuing systems, a DHU unit is placed to perform the damper header update; finally a damper is placed before each queuing system to remove the imposed jitter by the upstream switching fabric and queuing system. For example, the damper in the first switch compensates the jitter imposed by the queuing system of the source and the switching fabric of the first switch. Note that the propagation delay is constant and seen as a BDS. Here, the different clocks need not to be synchronized.

Example 2. Fig. 2 shows an example flow path within a large-scale deterministic network. Assume that the backbone network has relatively low delay (because of high-speed links, e.g. $100Gbps$ or more, worst-case delays tend to shrink [26]) and then the main source of jitter is the access network. For a given class of traffic, we want to remove the jitter imposed by the access network, in particular the forwarding plane and output queuing of each access router (each is treated as a JCS); therefore, each of these should have a DHU and a damper upstream of the output queuing system. In this example, the backbone network is modelled as a BDS; also, the source is unaware of any downstream damper and does not have a DHU and hence treated as a BDS. The jitter imposed by the access network is removed, but not the jitter caused by the backbone. The different clocks need not be synchronized and the backbone nodes are unmodified.

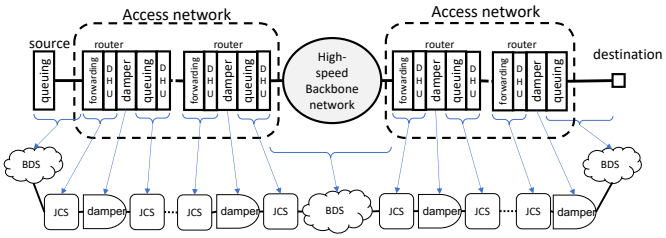

Fig. 2: A large-scale deterministic network example with no jitter removal at backbone network.

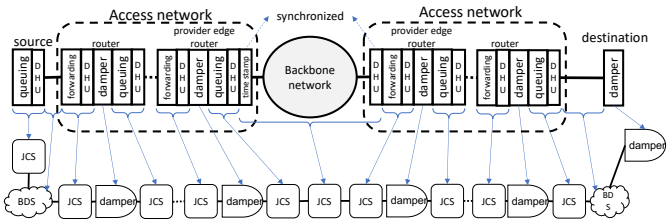

Fig. 3: A large-scale deterministic network example with jitter removal at backbone network.

Example 3. We continue in Fig. 3 with the previous example but assume now that, for some class of traffic with very low jitter requirement, the jitter induced by the backbone should be compensated. In such a case, we need to treat the backbone network as a JCS, i.e., we need to time stamp the arrival of each time-sensitive packet to the backbone and modify their damper header at the departure from the backbone. This can be done as in Fig. 3, where, at the upstream provider edge (PE) router, a time stamping unit should be added that inserts a field in the packet header equal to the departure time of each time-sensitive packet from the PE router in its local time (this operation can be done within the upstream DHU unit to avoid placement of a time-stamping unit); then at the egress downstream PE router, a DHU is placed that reads the departure time of the packet from packet header, removes it from packet header, computes earliness with its local clock and finally modifies the damper header. In this case, differently from previous examples, the time stamping and DHU are performed with different clocks; therefore, the PE routers should be time-synchronized, as otherwise the computation of earliness is impossible (time synchronization is never absolute

and, in sections III-B and IV-C, we analyze how to account for clock non-idealities). The jitter induced by the backbone network is compensated in the damper placed in the downstream PE router and hence removed. The PE routers must be time-synchronized (in provider networks, they typically are); backbone nodes are unmodified but deterministic packets carry an additional header for timestamps.

B. Assumptions on the Clocks

We call $\mathcal{H}_{\mathrm{TAI}}$ the perfect clock, i.e. the international atomic time (TAI[2]). In practice, the local clock of a system deviates from the perfect clock [24]. Typically the JCSs upstream of a damper operate with different clocks than the damper itself, and this can affect the performance of the damper as we see in Section V. In time-sensitive networks, clocks can be synchronized or non-synchronized. Non-synchronized clocks are independently configured and do not interact with each other; this corresponds to the *free-running* mode in [27, Section 4.4.1]. When clocks are synchronized, using methods like Network Time Protocol (NTP) [28], Precision Time Protocol (PTP) [29], WhiteRabbit [30], Global Positioning System (GPS) [31], the occurrence of an event, when measured with different clocks, is bounded by the *time error bound* ($\sim 1\mu$s or less in PTP, WhiteRabbit, and GPS; ~ 100 ms in NTP).

We follow the clock model in [24], which applies to time-sensitive networks. Consider a clock $\mathcal{H}_i$ that is either synchronized with time error bound ω, or not synchronized (in which case we set $\omega = +\infty$). Let $d^{\mathcal{H}_i}$ [resp. $d^{\mathcal{H}_{\mathrm{TAI}}}$] be a delay measurement done with clock $\mathcal{H}_i$ [resp. in TAI], then [24]:

$$\begin{aligned} d^{\mathcal{H}_{\mathrm{TAI}}} - d^{\mathcal{H}_i} &\leq \min\left((\rho-1)d^{\mathcal{H}_i} + \eta, 2\omega\right), \\ d^{\mathcal{H}_{\mathrm{TAI}}} - d^{\mathcal{H}_i} &\geq -\min\left(\left(1-\frac{1}{\rho}\right)d^{\mathcal{H}_i} + \frac{\eta}{\rho}, 2\omega\right), \end{aligned} \tag{1}$$

where ρ is the *stability bound* and η the *timing-jitter bound* of the clock $\mathcal{H}_i$. Note that this set of bounds is symmetric, i.e. we can exchange the roles of $\mathcal{H}_i$ and $\mathcal{H}_{\mathrm{TAI}}$ in (1). We assume that the parameters ω, ρ, η are valid for all clocks in the network, i.e. we consider network-wide time-error, stability and time-jitter bounds. When a flow has $\alpha^{\mathcal{H}_i}$ as arrival curve with clock $\mathcal{H}_i$, then an arrival curve in TAI is [24]:

$$\alpha^{\mathcal{H}_{\mathrm{TAI}}} : t \to \alpha^{\mathcal{H}_i}\left(\min\left\{\rho t + \eta, t + 2\omega\right\}\right). \tag{2}$$

In a TSN network, $\rho - 1 = 10^{-4}$ [32, Annex B.1.1] and $\eta = 2$ns [32, Annex B.1.3.1]]; if the network is synchronized with gPTP (generic PTP) then $\omega = 1\mu$s [32, Section B.3] and if it is not synchronized then $\omega = +\infty$.

C. Delay Jitter

For a given flow, call d_n the delay of packet n, measured in TAI. The "worst-case delay" of the flow is $\max_n\{d_n\}$ where the max is over all non-lost packets sent by the flow during its lifetime. Similarly, the "best-case delay" of the flow is $\min_n\{d_n\}$. The "delay jitter" (also called "jitter") is the difference, i.e., $V = \max_n\{d_n\} - \min_m\{d_m\}$, so that $d_m - d_n \leq V$ for any m, n. Delay jitter is called IP Packet Delay Variation in RFC 3393 [33].

[2]Temps Atomique International

IV. Taxonomy of Dampers

As mentioned earlier, designing a damper is a challenge and there exist very different implementations. In this section we classify such implementations in a manner that will be useful for our timing analysis. In the rest of this paper we call "eligibility time" the time at which a damper releases a packet, as in most implementations the packet is not actually moved, but simply made visible to the next processing element.

A. Dampers without FIFO constraint

An *ideal* damper delays a packet by exactly the amount required by the damping header. Consider a packet n with damper header H_n that arrives at local time Q_n to a damper. The theoretical eligibility time $\tilde{E}_n$ for the packet is:

$$\tilde{E}_n = Q_n + H_n, \tag{3}$$

and the ideal damper releases the packet at time $\tilde{E}_n$. Jitter-control EDF [15] is an ideal damper, used in combination with an EDF scheduler.

Many other implementations of dampers use some tolerance for the packet release times, due to the difficulty of implementing exact timings. We call damper *with tolerances* $(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}})$ a damper such that the actual eligibility time E_n, of packet n, in local time, satisfies:

$$\tilde{E}_n - \Delta^{\mathrm{L}} \leq E_n \leq \tilde{E}_n + \Delta^{\mathrm{U}}. \tag{4}$$

The tolerances can vary from hundreds of nanosecond to a few microsecond based on implementation. Hereafter, we study two instances of dampers with tolerances $(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}})$, namely, RCSP [16] and RGCQ [22].

RCSP is an implementation of a damper in relation with static-priority scheduler; each queue of the scheduler is implemented as a linked list and the damper is implemented as a set of linked lists and a calendar queue [34]. A calendar queue contains a clock and a calendar where each calendar entry points to an array of linked lists (each for one priority queue). The clock ticks every fix interval Δ. On each clock tick, the linked list that the current clock time of the calendar points is appended to the corresponding priority queue of the scheduler. Whenever a packet n arrives, its theoretical eligibility time is computed based on (3); then the actual eligibility time of the packet, $E_{n,\mathrm{RCSP}}$, is computed by rounding down the theoretical eligibility time, $E_{n,\mathrm{RCSP}} = \Delta\lfloor\frac{\tilde{E}_n}{\Delta}\rfloor$. Then, if $E_{n,\mathrm{RCSP}}$ is equal to the current clock time, it is appended to the corresponding priority queue of the scheduler; otherwise, it is appended to the linked list that the entry $E_{n,\mathrm{RCSP}}$ of the calendar points to. The computation of theoretical eligibility time is done with some errors in acquiring true local-time on packet arrival and in computation due to finite precision arithmetic that is bounded by ε (typically, in the order of a few nanoseconds). We can see that E_{RCSP} satisfies (4) when $(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}}) = (\Delta + \varepsilon, \varepsilon)$.

RGCQ, inspired by the idea of Carousel [35], is an implementation of a damper combined with a queuing system of a scheduler; in other words, each queue of a scheduler is replaced with an RGCQ. An RGCQ consists in a timer and

a set of gate-control queues (GCQs). By default, the GCQs are closed and are assigned unique increasing *openTime*s with interspacing of Δ. A GCQ is opened whenever the timer reaches to its openTime and is closed after it is emptied or being opened for a fixed amount of *expiration* time; when a GCQ is closed, its openTime is set as the largest openTime+Δ. The scheduler selects a packet for transmission from an open GCQ with smallest openTime. Whenever a packet n arrives, its theoretical eligibility time is computed based on (3); then the actual eligibility time of the packet, $E_{n,\mathrm{RGCQ}}$, is computed by rounding up the theoretical eligibility time, i.e., $E_{n,\mathrm{RGCQ}} = \Delta\lceil\frac{\tilde{E}_n}{\Delta}\rceil$. Then, the packet is enqueued to the GCQ whose openTime is $E_{n,\mathrm{RGCQ}}$. Similarly to RCSP, due to timing acquisitions and arithmetic rounding bounded by ε, we see that E_{RGCQ} satisfies (4) when $(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}}) = (\varepsilon, \Delta+\varepsilon)$.

B. Dampers with FIFO constraint

The definition of damper with tolerance given in the previous section does not mention whether the damper preserves packet order, and the satisfaction of (4) does not preclude packet misordering. Indeed, we show in Section VI that our two examples of dampers with tolerance, namely RCSP and RGCQ, can cause packet misordering due to clock non-idealities. Such a behavior is not possible with a class of proposed damper designs, which enforce the FIFO constraint, and which we now cover.

1) Re-sequencing damper: We call *re-sequencing damper* with tolerances $(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}})$ a system that behaves as the concatenation of a damper with same tolerances and a re-sequencing buffer that, if needed, re-orders packets based on the packet order at the entrance of the damper. The packet order is with respect to a flow of interest.

Formally, a system is a re-sequencing damper if there exists a sequence $\bar{E}_n$ such that the release times for the flow of interest, in local time, satisfy:

$$\begin{aligned} \tilde{E}_n - \Delta^{\mathrm{L}} \leq \bar{E}_n \leq \tilde{E}_n + \Delta^{\mathrm{U}}, \\ E_1 = \bar{E}_1, \quad E_n = \max\left\{\bar{E}_n, E_{n-1}\right\}, \end{aligned} \tag{5}$$

where $\tilde{E}_n$ is the theoretical eligibility time defined in (3) and packet numbers $n = 1, 2, ...$ are in order of arrival at the damper.

It follows that such a damper is FIFO for the flow of interest and that[3]:

$$\max_{i\leq n}\left\{\tilde{E}_i\right\} - \Delta^{\mathrm{L}} \leq E_n \leq \max_{i\leq n}\left\{\tilde{E}_i\right\} + \Delta^{\mathrm{U}}. \tag{6}$$

We say that a re-sequencing damper is *ideal* if has zero tolerances. Hereafter, we describe two instances of re-sequencing dampers, namely, SCED+ [17] and FOPLEQ [23].

SCED+ is an implementation of a damper in combination with SCED scheduling. The damper in [17] is defined as a conceptual element with tolerance Δ. Accordingly, each packet is assigned an initial eligibility time and a terminal eligibility time where the difference between the two is Δ. In SCED+, the damper ensures that the damper is released after the initial eligibility time and before the terminal eligibility time. In fact, the dampers assigns a tentative eligibility time, $\bar{E}_n$ to a packet n, where:

$$\tilde{E}_n - \Delta \leq \bar{E}_n \leq \tilde{E}_n. \tag{7}$$

SCED+ assumes that the damper serves packets in FIFO manner; then, the actual eligibility time of the packet n is:

$$E_1 = \bar{E}_1, \quad E_n = \max\left\{\bar{E}_n, E_{n-1}\right\}; \quad n \geq 2. \tag{8}$$

so that SCED+ is a re-sequencing damper with tolerances $(\Delta+\varepsilon, \varepsilon)$, where ε is a bound on the errors on timing acquisition and arithmetic rounding.

FOPLEQ, similarly to RGCQ, is inspired by the architecture of Carousel [35]. Accordingly, it has a set of time-based queues along with a table, called eligibility time table (ETT), for the purpose of preserving the order of packets inside FOPLEQ. Each row in ETT belongs to a flow that has a packet in the Carousel and stores a tentative eligibility time of the latest packet belonging to the corresponding flow. The tentative eligibility time of a packet is obtained by dividing its theoretical eligibility time by Δ and rounding down the computed value. Consider a packet n of the flow of interest, where number is in the order of arrival at the FOPLEQ. First a theoretical eligibility time is computed using (3); second, a tentative eligibility time is obtained by rounding down to a multiple of Δ, i.e. $\bar{E}_n = \Delta\lfloor\frac{\tilde{E}_n}{\Delta}\rfloor$; then, the actual eligibility time of the packet is the maximum of its tentative eligibility time and the stored tentative eligibility time of the flow of interest in the ETT. The tentative eligibility times correspond to a damper with tolerances $(\Delta+\varepsilon, \varepsilon)$, where ε is a bound on the errors on timing acquisition and arithmetic rounding, and therefore FOPLEQ is a re-sequencing damper with tolerances $(\Delta+\varepsilon, \varepsilon)$.

2) Head-of-line (HoL) damper: The idea is introduced in [21]. A HoL damper is implemented as a FIFO queue. When a packet arrives, its arrival time is collected and the packet is stored at the tail of the queue. Only the packet at the head of the queue is examined; if its eligibility time is passed, it is immediately released, otherwise it is delayed and released at its eligibility time. When the head packet is released, it is removed from the damper queue and the next packet (if any) becomes the head of the queue and is examined. When an arriving packet finds an empty queue, it is immediately examined. By construction, packet ordering is preserved.

As before, the model should incorporate some tolerance to account for the timing inaccuracy and for processing times. Unlike with previous damper models, these two things cannot be aggregated because the head-of-line property has the effect that processing times may have an effect over subsequent packets (this is visible in Theorem 4).

Formally, we model a head-of-line damper as follows. It has tolerance parameters $\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}}$ that account for the accuracy of timings, as well as processing bounds $\phi^{\min}, \phi^{\max}$ that account for non-zero processing times. We must have $\Delta^{\mathrm{L}} \geq 0, \Delta^{\mathrm{U}} \geq 0$ and $0 \leq \phi^{\min} \leq \phi^{\max}$. Packet numbering is with respect to the order of arrivals at the damper and is global for this damper

[3]The converse does not hold, i.e., any system that is FIFO for the flow of interest and satisfies (6) is not necessarily a re-sequencing damper.

(not per-flow). We say that a system is a head-of-line damper if the release times E_n, in local time, satisfy:

$$\begin{aligned}\tilde{E}_1 - \Delta^{\mathrm{L}} \leq E_1 \leq \tilde{E}_1 + \Delta^{\mathrm{U}},\\ \max(\tilde{E}_n - \Delta^{\mathrm{L}}, E_{n-1}) + \phi^{\min} \leq E_n\\ \leq \max(\tilde{E}_n + \Delta^{\mathrm{U}}, E_{n-1}) + \phi^{\max},\end{aligned} \tag{9}$$

where $\tilde{E}_n$ is the theoretical eligibility time as in (3).

The definition in (9) can be explained as follows. First, the eligibility times are obtained with some errors due to timing acquisition and arithmetic rounding. Let $\bar{E}_n$ be the resulting tentative eligibility times, so that

$$\tilde{E}_n - \Delta^{\mathrm{L}} \leq \bar{E}_n \leq \tilde{E}_n + \Delta^{\mathrm{U}}. \tag{10}$$

Second, packet n is examined only when packet $n-1$ is released, and this action takes a processing time $\phi_n \in [\phi^{\min}, \phi^{\max}]$. The actual release time is therefore

$$E_n = \max(\bar{E}_n, E_{n-1}) + \phi_n. \tag{11}$$

Using Lemma 2 in Appendix A-A with $a = E_{n-1}$, $x^{\min} = \phi^{\min}$, $x^{\max} = \phi^{\max}$, $y^{\min} = \tilde{E}_n - \Delta^{\mathrm{L}}$, $y^{\max} = \tilde{E}_n + \Delta^{\mathrm{U}}$, $x = \phi_n$, $y = \bar{E}_n$ and $z = E_n$ we obtain that (10) and (11) imply (9); conversely, if (9) holds, there exists sequences $\bar{E}_n$ and $\phi_n \in [\phi^{\min}, \phi^{\max}]$ such that (10) and (11) hold.

If the tolerances and processing bounds are all equal to 0, then the HoL damper is called *ideal*. It follows immediately from (9) and (5) that an ideal HoL damper is the same as an ideal re-sequencing damper.

In [21], Jitter-control ATS is presented as an ideal head-of-line damper in combination with Asynchronous Traffic Shaping [20] within a switch where each FIFO queue is shared among all time-sensitive flows that come from the same input port, have the same class, and go to the same output port. In [21], the authors implicitly assume that the tolerances and processing times are zero and therefore ignore them in their analysis. This assumption might not hold in practical cases, specifically when a large number of packets become eligible at the same time in a jitter-control ATS. The effect of non-zero tolerances and processing times appear in Theorem 4 and is illustrated numerically in Section VIII.

C. Damper Header Computation

In this subsection, we first describe the operation of damper header update unit. Then, we discuss the possible sources of error in the computation.

1) DHU unit operation: The DHU unit of a JCS computes the earliness of a packet and updates the damper header. A classical approach to compute the earliness is to first measure the actual delay of the packet in the JCS with the clock of DHU unit; then set the earliness as the difference between the known delay bound δ of the system for this class of traffic and the actual delay of the packet [15], [16]. More precisely, for a packet n, its arrival time is time stamped with local clock $\mathcal{H}_{\mathrm{TS}}$ and stored locally (Examples 1 and 2 in Section III-A) or delivered by the packet (Example 3 in Section III-A); let $\tilde{A}_n^{\mathcal{H}_{\mathrm{TS}}}$ denote the stored/delivered value. Then the DHU unit time stamps the departure time of the packet with its local clock $\mathcal{H}_{\mathrm{DHU}}$; let $\tilde{W}_n^{\mathcal{H}_{\mathrm{DHU}}}$ denote the departure time. Then, the DHU unit computes the earliness of the packet as

$$\mathrm{earliness}_n = \delta - \left(\tilde{W}_n^{\mathcal{H}_{\mathrm{DHU}}} - \tilde{A}_n^{\mathcal{H}_{\mathrm{TS}}}\right). \tag{12}$$

The last step for the DHU unit is to update the damper header that is equal to the current damper header incremented by the computed earliness, and write the result in the damper header field. Then the packet leaves the JCS. In the case that the JCS is connected to an output link, the departure time of a packet is the complete packet transmission and thus the packet header is accessible to write the damper header just before packet transmission. Therefore, the start of transmission time of the packet is time stamped ($T_n^{\mathcal{H}_{\mathrm{DHU}}}$) and the transmission time is inferred as $\tilde{\tau}_n^{\mathcal{H}_{\mathrm{DHU}}} = \left\{\frac{l_n}{c}\right\}^{\mathcal{H}_{\mathrm{DHU}}}$ with l_n as the packet length and c as the transmission rate. Then, we set the departure time to $\tilde{W}_n^{\mathcal{H}_{\mathrm{DHU}}} = T_n^{\mathcal{H}_{\mathrm{DHU}}} + \tilde{\tau}_n^{\mathcal{H}_{\mathrm{DHU}}}$ and compute the earliness using (12). This method of damper header computation is used in most of the existing damper variants like RCSP [16], FOPLEQ [23] and jitter-control ATS [21]. We call this the *default* method of damper header computation.

Recently, [22] proposed a subtle change in the computation of earliness when a JCS comes immediately after a damper with tolerances $(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}})$. In particular, they suggest to time stamp the theoretical eligibility time $\tilde{E}_n$ of packet from the damper instead of the arrival time to the JCS; as a consequence, the jitter imposed by the tolerance of the damper is compensated by the next upstream damper. In such proposal, note that the delay upper-bound between the theoretical eligibility time to the arrival time to the JCS (i.e., the actual eligibility time from the damper) should be added to the earliness; by (4), this upper bound is Δ^{U}. Hence, the earliness for theoretical eligibility time stamping is:

$$\mathrm{earliness}_n = \delta + \Delta^{\mathrm{U}} - \left(\tilde{W}_n^{\mathcal{H}_{\mathrm{DHU}}} - \tilde{A}_n^{\mathcal{H}_{\mathrm{TS}}}\right). \tag{13}$$

We call this method of damper header computation *TE time-stamping*.

2) Errors in damper header computation: The DHU unit computes a damper header equal to the current damper header incremented by the computed earliness, and write the result in the damper header field. This step is imperfect due to finite precision arithmetic and finite resolution of the damper header. The corresponding error is $e_{\mathrm{update},n} = H_n - \tilde{H}_n$, where $\tilde{H}_n$ is the theoretical value of the damper header and H_n is the actual value written in the packet.

In the computation of earliness ((12) and (13)), when $\tilde{A}_n^{\mathcal{H}_{\mathrm{TS}}}$ is delivered within a packet header field (Example 3 in Section III-A), there is some error induced due to the finite resolution of the header field. The corresponding error is $e_{\mathrm{ts},n} = A'^{\mathcal{H}_{\mathrm{TS}}}_n - \tilde{A}_n^{\mathcal{H}_{\mathrm{TS}}}$, where $A'^{\mathcal{H}_{\mathrm{TS}}}_n$ is the time stamped value at the packet arrival to the JCS.

As discussed earlier, when the JCS is connected to a transmission link, the DHU unit can infer the transmission time by dividing the packet length over the nominal transmission rate of the link. Due to transmission of preamble and inexact knowledge of actual transmission rate, the inference of transmission time is done with some error $e_{\mathrm{tran},n} = \tilde{\tau}_n^{\mathcal{H}_{\mathrm{DHU}}} - \tau_n^{\mathcal{H}_{\mathrm{DHU}}}$, where $\tau_n^{\mathcal{H}_{\mathrm{DHU}}}$ and $\tilde{\tau}_n^{\mathcal{H}_{\mathrm{DHU}}}$ are the actual

and inferred transmission times. The error $e_{\mathrm{tran},n}$ can go up to tens of nanoseconds [36], [37].

Acquiring the true local-time on packet arrival and within the DHU unit usually comes with an error. We define the clock acquisition error as: $e_{\mathrm{acq},n} = \left(W_n^{\mathcal{H}_{\mathrm{DHU}}} - \tilde{W}_n^{\mathcal{H}_{\mathrm{DHU}}}\right) + \left(A_n^{\mathcal{H}_{\mathrm{TS}}} - A'^{\mathcal{H}_{\mathrm{TS}}}_n\right)$, where $A_n^{\mathcal{H}_{\mathrm{TS}}}$ and $W_n^{\mathcal{H}_{\mathrm{DHU}}}$ are the true local times on packet arrival and departures.

The two clocks $\mathcal{H}_{\mathrm{DHU}}$ and $\mathcal{H}_{\mathrm{TS}}$ are often the same (Examples 1 and 2 in Section III-A), but not always (Example 3 in Section III-A). We select $\mathcal{H}_{\mathrm{DHU}}$ as the reference clock of a JCS to compute damper header; then we define the error with respect to the reference clock as: $e_{\mathrm{clk},n} = A_n^{\mathcal{H}_{\mathrm{DHU}}} - A_n^{\mathcal{H}_{\mathrm{TS}}}$, where $A_n^{\mathcal{H}_{\mathrm{DHU}}}$ is the time that would be displayed at packet arrival if $\mathcal{H}_{\mathrm{DHU}}$ would be used. If the clocks are the same, $e_{\mathrm{clk}} = 0$; if the clocks are synchronized with error ω with respect to TAI, $|e_{\mathrm{clk}}| \leq 2\omega$; and finally if the clocks are not synchronized, e_{clk} can get arbitrary large, which is incompatible with the goal of removing jitter. Therefore, in this paper, we assume that both clocks $\mathcal{H}_{\mathrm{TS}}$ and $\mathcal{H}_{\mathrm{DHU}}$ are either one and the same, or are synchronized.

To summarize, the value of a damper header, as written in a packet n, suffers from some error e_n equal to: $e_n = e_{\mathrm{update},n} + e_{\mathrm{ts},n} + e_{\mathrm{tran},n} + e_{\mathrm{acq},n} + e_{\mathrm{clk},n}$. Each of these sources of error can be bounded, depending on the technology used by the routers and switches. The variable ϵ denotes an upper bound on the error e_n, i.e., $|e_n| \leq \epsilon$. When $\mathcal{H}_{\mathrm{DHU}}$ and $\mathcal{H}_{\mathrm{TS}}$ are the same, ϵ is typically of the order of tens of nanoseconds; if they are synchronized, ϵ is mainly dominated by the time error bound (e.g. $\epsilon = 2$ μs for gPTP).

V. Delay Analysis of Dampers without FIFO constraints

In this section we study the end-to-end delay and jitter of a flow when dampers without FIFO constraint are used. The first step is to decompose a flow path into a set of blocks that can be analyzed separately. Every block is as in Fig. 4; it contains a number of JCSs and BDSs and ends in a damper with tolerance. The second step, given in the rest of this section, is to give delay and jitter bounds for a flow through such a block. The bounds are valid whether the JCSs and the BDSs of the block are FIFO or not. The last step, to obtain end-to-end results, simply consists in summing up the delays and jitters of every block and, possibly, of remaining BDSs. For example, in Fig. 2, from source to the first router and from the queuing system of the last router to the destination are BDSs and the rest are decomposed in blocks as in Fig. 4.

In the following we give delay and jitter bounds for a block as in Fig. 4. Theorem 1 gives the result for dampers without FIFO constraint when the default mode of header computation is used (as explained in Section IV-C) and Theorem 2 when TE time-stamping is used. In both cases, we capture the effect of errors and non-ideal clocks. We also illustrate cases where the errors and non-ideal clocks make a major contribution to the jitter bound.

Theorem 1. *Consider a flow of interest that traverses the block in Fig. 4. The block contains a sequence of JCSs and BDSs and terminates in a damper with tolerances* $(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}})$. *Assume that the clock of every system has stability bound* ρ, *timing-jitter bound* η *and time-error bound* ω *with respect to TAI (Section III-B). Assume that JCS* i *has a delay upper bound* δ_i, *which is used for damper header computation, in its local time. Also, assume that the BDS* j *has delay lower and upper bounds* $\underline{\pi}_j^{\mathcal{H}_{\mathrm{TAI}}}$ *and* $\overline{\pi}_j^{\mathcal{H}_{\mathrm{TAI}}}$ *and jitter bound* $\nu_j^{\mathcal{H}_{\mathrm{TAI}}}$, *all in TAI. Then, the delay of a packet from entrance to the exit of the block, in TAI, is upper-bounded by* $\overline{D}$, *low-bounded by* $\underline{D}$ *and has jitter bound* V, *with*

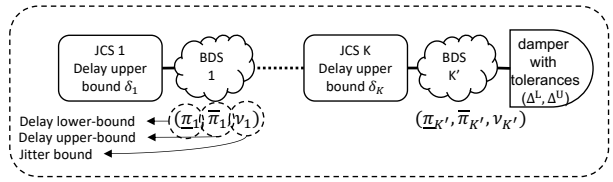

Fig. 4: Structure of a block whose delay and jitter bounds are computed in Theorem 1.

$$\overline{D} = \sum_{j=1}^{K} \delta_j + \sum_{j=1}^{K'} \overline{\pi}_j^{\mathcal{H}_{\mathrm{TAI}}} + \Delta^{\mathrm{U}} + K\epsilon + \overline{\psi},$$

$$\underline{D} = \sum_{j=1}^{K} \delta_j + \sum_{j=1}^{K'} \underline{\pi}_j^{\mathcal{H}_{\mathrm{TAI}}} - \Delta^{\mathrm{L}} - K\epsilon - \underline{\psi},$$

$$V = \sum_{j=1}^{K'} \nu_j^{\mathcal{H}_{\mathrm{TAI}}} + \Delta^{\mathrm{U}} + \Delta^{\mathrm{L}} + 2K\epsilon + \overline{\psi} + \underline{\psi},$$

where $\overline{\psi}$ *and* $\underline{\psi}$ *are due to clock non-idealities,*

$$\overline{\psi} = \min\Big((\rho - 1)(\Delta^{\mathrm{U}} + \sum_{j=1}^{K}(\delta_j + \epsilon)) + (K+1)\eta \\ , 2(K+1)\omega\Big),$$

$$\underline{\psi} = \min\Big((1 - \frac{1}{\rho})(-\Delta^{\mathrm{L}} + \sum_{j=1}^{K}(\delta_j - \epsilon)) + \frac{(K+1)\eta}{\rho} \\ , 2(K+1)\omega\Big). \tag{14}$$

The bounds are tight, i.e., for any tolerances $(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}})$, *every* δ_i, *any* $\underline{\pi}_j^{\mathcal{H}_{\mathrm{TAI}}}$, $\overline{\pi}_j^{\mathcal{H}_{\mathrm{TAI}}}$, $\nu_j^{\mathcal{H}_{\mathrm{TAI}}}$, *there is a system and two individual execution traces such that in one of them a packet experiences a delay of* $\overline{D}$ *and in the other one a packet experiences a delay of* $\underline{D}$.

The proof is in Appendix A-B.

Remark. The second arguments of the $\min(,)$ functions in (14) capture the impact of clock time error bounds when all the $K+1$ clocks (K JCSs and one damper with tolerance) are different from each other. If some systems share a common clock, so that there are $X \leq K$ different clocks in total, the second argument of the $\min(,)$ functions should be replaced by $2(X+1)\omega$.

Hereafter, we provide an application of Theorem 1 to obtain delay and jitter bounds for the three examples of Section III-A. Then we compare the bounds with the *basic* bounds obtained

when assuming that clocks are perfect, i.e. by summing the tolerances of dampers and the jitters of BDSs.

Example 1. Consider Example 1 in Section III-A for a flow that traverses 6 switches. Assume that the switching fabrics (as JCSs) have a delay upper-bound of 2 μs and the delay bound at each queuing system (as a JCS) is 250 μs. Suppose that the error $\epsilon = 50$ ns and all the dampers are RCSP with $(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}}) = (1\ \mu\mathrm{s}, 2\ \mathrm{ns})$. Assume the propagation delay (as a BDS) is fixed and equal to 5 μs for all links. Assume first that the clocks of the switches are not synchronized, i.e. we set the time-error bound ω to ∞ in (14). Then, by applying Theorem 1 from source to the output of the first damper, the delay upper-bound is $\overline{D} = 257.13\ \mu$s; the delay jitter is $V = 1.262\ \mu$s of which 200 ns is due to errors and 62 ns is due to non-ideal clocks. The basic jitter bound is $1.002\ \mu$s and is due to the tolerance of the first damper. We can see that the error and non-ideal clocks add 262 ns (26%) to the basic jitter bound. The end-to-end delay and jitter bounds are computed by summing up the delay and jitter bounds from the output of one damper to the output of the next downstream damper until the destination; this gives an end-to-end delay upper-bound of 1.799 ms and end-to-end jitter bound of $8.834\ \mu$s. The values remain the same if we assume next that the clocks of the switches are synchronized with a time-error bound of 1 μs, as is typical in IEEE TSN systems.

Example 2. Consider Example 2 in Section III-A for a flow that traverses four access routers to reach the backbone and traverses four other access routers to reach to the destination. Assume that 1) the queuing delay at source has a delay upper-bound of 100 μs and the jitter bound of 80 μs, 2) the delay upper-bound at the output queuing and packet forwarding of each access router are 500 μs and 5 μs and the output queuing has jitter of 100 μs, 3) the backbone network has a delay upper-bound of 30 ms and jitter bound of 1 ms, 4) the propagation delay is 10 μs, 5) the error $\epsilon = 50$ ns and 6) all dampers are RCSP with $(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}}) = (1\ \mu\mathrm{s}, 2\ \mathrm{ns})$. Then, by using Theorem 1, the end-to-end delay upper-bound is $\overline{D}_{\mathrm{e2e}} = 34.211$ ms; delay jitter is $V_{\mathrm{e2e}} = 1.190$ ms of which 1.5 μs is due to the errors and 800 ns is due to non-ideal clocks. The basic jitter bound is 1.188 ms that is due to the tolerance of the dampers, as well as the BDSs, i.e., the backbone network, the source output queuing and the output queuing of the last access router (before the destination). We can see that here the effect of the errors and non-ideal clocks is negligible due to the jitter of the BDSs captured by the basic jitter bound.

Example 3. Consider Example 3 in Section III-A for a flow that traverses four access routers to reach the backbone and traverses four other access routers to reach to the destination. Also, consider the same numerical assumptions as the previous example. We want to remove jitter of the backbone network using time stamping at the upstream PE router. Assume that the PE routers are synchronized with error bound of 1 μs; hence the error damper header computation at the downstream PE router of the backbone network is bounded by 2.05 μs (the error at the other JCSs is bounded by 50 ns). Then, by using Theorem 1, the end-to-end delay upper-bound is $\overline{D}_{\mathrm{e2e}} = 34.216$ ms; delay jitter is $V_{\mathrm{e2e}} = 21.74\ \mu$s of which 5.8 μs is due to the errors and 6.92 μs is due to non-ideal clocks. Comparing to the previous example, the basic jitter bound is reduced to 9.02 μs as the jitter of the backbone network, queuing at source and the queuing at the last access router are removed. We can see that the errors and clock non-idealities add 12.72 μs (141%) to the basic jitter bound.

TABLE I: Minimum values of the sum of delay bounds for the JCSs within a block such that clock synchronization improves the delay and jitter bounds in Theorem 1.

Synchronization method	Time-error bound (ω)	Minimum value of $\sum_{j=1}^{K} \delta_j$
White Rabbit	100ns	3.96ms
gPTP	1μs	39.96ms
NTP	100ms	3.99s

We see from these examples that, when the remaining end-to-end delay-jitter is still large after applying dampers (ms or more, Example 2) then the timing errors and clock non-idealities do not play a significant role and can be ignored. In contrast, for very small residual delay-jitter (Examples 1 and 2, 10 μs or less), ignoring timing errors and clock non-idealities can lead to significant under-estimation.

Remark. In Example 1, we see that the delay-jitter bound is not affected by the time-error bound, i.e., here, time synchronization does not improve the performance of dampers. We can easily analyze when this is the case, by comparing the terms in the $\min(.)$ functions in (14). We find that time synchronization does not improve the performance of dampers if and only if

$$\sum_{j=1}^{K} \delta_j \leq \frac{K+1}{\rho-1}\left(2\omega - \eta\right) - \Delta^{\mathrm{U}} - K\epsilon. \tag{15}$$

It follows that if $\sum_{j=1}^{K} \delta_j > \frac{2}{\rho-1}\left(2\omega - \eta\right)$, the time error bound affects the delay and jitter bounds of Theorem 1; i.e., it is the relation between the delay (not delay-jitter) bound and the time-error bound that matters (see Table I).

TSN networks are typically synchronized with gPTP ($\omega = 1\ \mu$s) [32, Section B.3]. Three main delay sensitive classes are Control-Data Traffic (CDT), class A for audio traffic and class B for video traffic. According to TSN documents [6], [12], [38], the end-to-end delay requirement for CDT, classes A and B are respectively 100 μs in 5 hops, 2 ms and 50 ms in 7 hops. According to Table I, the gPTP synchronization does not impact the obtained delay bound using Theorem 2 for CDT and class A. For class B, if we consider that for each block the sum of JCS delay bounds is less than 39.96 ms, similarly the gPTP synchronization does not play a role. This implies when all switches and the destinations in a TSN network implement dampers with tolerances and the source performs time stamping (as a JCS), then without gPTP synchronization the same performance is achieved.

In order to provide delay and delay-jitter guarantees to time-sensitive flows, it is often required to bound the burstiness of flows inside the network, which is typically larger than at the source. Finding such bounds may be difficult, and worst-case bounds may be large when there are cyclic dependencies

[39]. Here, dampers can help a lot, as shown by the following Corollary, which comes by direct application of the jitter bound in Theorem 1 and [18, Lemma 1].

Corollary 1. *Consider Fig. 4. Suppose that a flow has $\alpha^{\mathcal{H}_{\rm TAI}}$ as arrival curve at the entrance of the block. Then an arrival curve at the output of the block, in TAI, is given by $\alpha_h^{\mathcal{H}_{\rm TAI}}(t) = \alpha^{\mathcal{H}_{\rm TAI}}(t+V)$ where V is the jitter bound of the block defined in Theorem 1.*

Example. In Example 1 of Section III-A, suppose that the flow has leaky bucket arrival curve with rate 16 Mbps, in TAI, and burstiness 10 KBytes at source. We computed that the jitter bound is 1.262 μs from source the output of the first damper. Then the arrival curve at the output of the first damper has the same rate and the burstiness is increased by 3 Bytes. Without damper, the burstiness increase would be 515 Bytes: we see that the burstiness increase due to multiplexing is almost entirely removed.

Remark. The arrival curve constraint at source may be available in its local time rather than in TAI. Then, we can apply (2), to obtain an arrival curve in TAI and then use the result of Corollary 1.

When dampers use TE time-stamping for damper header computation rather than the default method, the delay and jitter bounds computation with TE time-stamping are slightly different than in Theorem 1. A JCS is affected only when the upstream damper uses TE time-stamping (otherwise, the bounds are the same). The next theorem gives end-to-end delay and jitter bounds when DHU unit uses TE time-stamping.

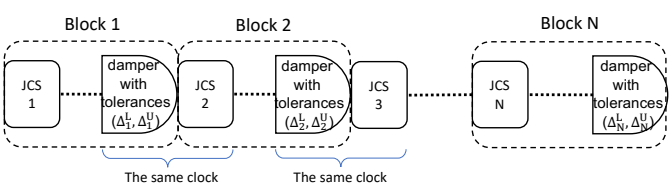

Fig. 5: The notations used in Theorem 2.

Theorem 2. *Consider Fig. 5 where a sequence of N blocks are concatenated and TE time-stamping is used for damper header computation. Assume that clocks follow the description in Section III-B and damper with tolerances at block i ($i = 1, \ldots, N-1$) and JCS $i+1$ operate with the same clock. Assume that there are M JCSs in total. Let us denote the the sum of the delay bounds of the JCSs as $\delta_{\rm e2e}$ and the sum of delay lower and upper bounds and jitter bound of the BDSs as $\underline{\pi}_{\rm e2e}, \overline{\pi}_{\rm e2e}$ and $\nu_{\rm e2e}$ respectively. Then,*

$$\overline{D}_{\rm TE} = \delta_{\rm e2e} + \overline{\pi}_{\rm e2e} + \sum_{j=1}^{N} \Delta_j^{\rm U} + M\epsilon + \overline{\Psi}_{\rm TE},$$

$$\underline{D}_{\rm TE} = \delta_{\rm e2e} + \underline{\pi}_{\rm e2e} + \sum_{j=1}^{N-1} \Delta_j^{\rm U} - \Delta_N^{\rm L} - M\epsilon - \underline{\Psi}_{\rm TE},$$

$$V_{\rm TE} = \nu_{\rm e2e} + \Delta_N^{\rm U} + \Delta_N^{\rm L} + 2M\epsilon + \overline{\Psi}_{\rm TE} + \underline{\Psi}_{\rm TE}, \qquad (16)$$

where $\overline{\Psi}_{\rm TE}$ and $\underline{\Psi}_{\rm TE}$ are the errors due to non-ideal clocks:

$$\overline{\Psi}_{\rm TE} = \min\Big((\rho-1)(\delta_{\rm e2e} + \sum_{i=1}^{N} \Delta_i^{\rm U} + M\epsilon) + (M+N)\eta, 2(M+N)\omega\Big),$$

$$\underline{\Psi}_{\rm TE} = \min\Big((1-\frac{1}{\rho})(\delta_{\rm e2e} - \Delta_N^{\rm L} + \sum_{i=1}^{N-1} \Delta_i^{\rm U} + M\epsilon) + \frac{(M+N)\eta}{\rho}, 2(M+N)\omega\Big). \qquad (17)$$

The proof is available in Appendix A-C.

Example. Let us redo the end-to-end delay and jitter bounds computation for the three examples of Section III-A using Theorem 2 and compare them with the ones obtained with Theorem 1. Let us consider the same assumptions made when applying Theorem 1. We can see that the delay upper-bounds obtained by Theorem 2 are the same as the ones computed after Theorem 1; however, the end-to-end jitter is reduced. Using Theorem 2, the end-to-end jitter bound for Example 1 is $V_{\rm Ex1} = 2.834$ μs, Example 2 is $V_{\rm Ex2} = 1.183$ ms, Example 3 is $V_{\rm Ex3} = 13.74$ μs. The reason for jitter bound reduction by Theorem 2 is the elimination of the jitter imposed by the tolerance of all the intermediate dampers by the next downstream dampers. In examples 1 and 3, the jitter bounds are considerably reduced, by 68% and 36%; however, this is not the case for Example 2 as the main sources of jitter are the BDSs. Furthermore, the jitter imposed by the errors and the non-ideal clocks incorporate 65% and 92% of the the end-to-end jitter bounds computed for examples 1 and 3, which are respectively 2.8 and 13.74 times the basic jitter bounds.

VI. Packet reordering in Dampers Without FIFO Constraints

In this Section we show that dampers without FIFO constraint can cause packet misordering, and we quantify the corresponding reordering metrics.

Obviously, a damper modifies packet order if the sequence of theoretical eligibility times is not monotonic. Since the theoretical eligibility time is equal to the arrival time at the JCS plus a constant, this may occur only if the packet order at the entrance to the damper is not the same as at the entrance to the JCS, i.e. this requires the JCS to be non FIFO. But, as we show next, this may occur even if the JCS is FIFO, due to timing inaccuracies.

RGCQ and RCSP are two instances of dampers with tolerance; by design, they avoid packet reordering due to the tolerances by enforcing FIFO behavior after computation of theoretical eligibility times. However, as we show next, packet reordering may still occur within RGCQ and RCSP due to the errors of damper header computation and non-ideal clocks.

Re-ordering example with RGCQ. Consider Fig. 6 where the damper is RGCQ with tolerances $(\Delta^{\rm L}, \Delta^{\rm U})$ and clocks are not synchronized. Assume that the JCS represents a FIFO queue connected to a transmission line with a fixed rate and the BDS has zero jitter and represents constant propagation delay (similar to the first hop in Example 1 of Section III-A).

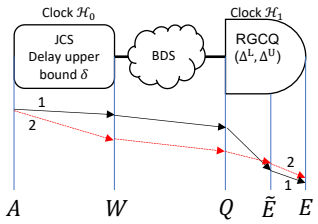

Fig. 6: Packet reordering scenario when two packets enter back-to-back to a JCS.

Suppose that two packets 1 and 2 enter the JCS at the same time while 1 is prior to 2. Then packet 1 leaves before packet 2. The damper headers in the packets are:

$$\begin{aligned} H_1 &= \delta - \tilde{\tau}_1^{\mathcal{H}_0}, \\ H_2 &= \delta - \tilde{\tau}_1^{\mathcal{H}_0} - \tilde{\tau}_2^{\mathcal{H}_0} = H_1 - \tilde{\tau}_2^{\mathcal{H}_0}, \end{aligned} \tag{18}$$

where $\tilde{\tau}_i^{\mathcal{H}_0}$ is the inferred transmission times of packets $i \in \{1, 2\}$ measured with $\mathcal{H}_0$. Then, the interspacing of the two packet at the output of the JCS is:

$$W_2^{\mathcal{H}_0} - W_1^{\mathcal{H}_0} = \tau_2^{\mathcal{H}_0}, \tag{19}$$

where $\tau_2^{\mathcal{H}_0}$ is the actual transmission time of packet 2 and $W_i^{\mathcal{H}_0}$ is the departure time of packet $i \in \{1, 2\}$ from the JCS. Both packets experience the same delay in the BDS. Therefore, the interspacing between the two packets at the entrance of RGCQ when seen with clock $\mathcal{H}_1$ is:

$$Q_2^{\mathcal{H}_1} - Q_1^{\mathcal{H}_1} = \tau_2^{\mathcal{H}_1} = \tau_2^{\mathcal{H}_0} + \left(\tau_2^{\mathcal{H}_1} - \tau_2^{\mathcal{H}_0}\right), \tag{20}$$

where $Q_i^{\mathcal{H}_1}$ is the arrival time of packet $i \in \{1, 2\}$ to RGCQ. Then, by (18) and (3), the difference between the theoretical eligibility times of packets 2 and 1 is:

$$\begin{aligned} \tilde{E}_2^{\mathcal{H}_1} - \tilde{E}_1^{\mathcal{H}_1} &= Q_2^{\mathcal{H}_1} - Q_1^{\mathcal{H}_1} + H_2 - H_1 \\ &= \left(\tau_2^{\mathcal{H}_0} - \tilde{\tau}_2^{\mathcal{H}_0}\right) + \left(\tau_2^{\mathcal{H}_1} - \tau_2^{\mathcal{H}_0}\right). \end{aligned} \tag{21}$$

The difference between the theoretical eligibility times is the sum of the error between actual and inferred transmission time and the measurement difference of packet 2 transmission time seen from clocks $\mathcal{H}_1$ and $\mathcal{H}_0$. Therefore, if it happens that clock $\mathcal{H}_1$ is faster than $\mathcal{H}_0$ during the transmission time of packet 2 from the JCS, then $\tau_2^{\mathcal{H}_1} < \tau_2^{\mathcal{H}_0}$, hence $\tilde{E}_2^{\mathcal{H}_1} - \tilde{E}_1^{\mathcal{H}_1} < 0$, i.e. packet 2 has smaller theoretical eligible time than packet 1. Then, by implementation of RGCQ discussed in Section IV, packet 2 leaves RGCQ before packet 1.

Remark. In this scenario, reordering occurs because of the difference of speed between the two clocks $\mathcal{H}_0$ and $\mathcal{H}_1$ at the microscopic scale and the error in inferring the transmission time. The earliness of a packet written in the header is measured using the local clock $\mathcal{H}_0$ while the delay imposed to the packet is measured in the RGCQ using the local clock $\mathcal{H}_1$. Even if both systems are time synchronized, there still remains a small difference in the time measurements performed by the two clocks. Over the transmission time of a packet, there is equal chance that one clocks ticks slightly faster than the other, i.e. there is 50% chance that the change of order described in this scenario occurs.

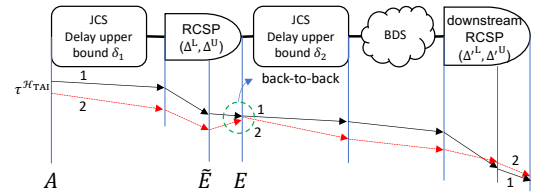

Fig. 7: A scenario that two packets become back-to-back after an RCSP and reordering occurs in the downstream RCSP.

Re-ordering example with RCSP. Consider Fig. 7 where the dampers are RCSP. Assume that the first JCS represents a router, the second JCS is a FIFO queue connected to a transmission line with a fixed rate and the BDS has zero jitter and represents a constant propagation delay; this resembles the first and second access routers in Example 2 of Section III-A. Now, focus on the first JCS and the first RCSP. Suppose two packets 1 and 2 enter the JCS with interspacing $\tau^{\mathcal{H}_{\mathrm{TAI}}}$, measured in TAI (e.g. transmission time of packet 2 from source, when packets are sent back-to-back from source), i.e.,

$$A_2^{\mathcal{H}_{\mathrm{TAI}}} - A_1^{\mathcal{H}_{\mathrm{TAI}}} = \tau^{\mathcal{H}_{\mathrm{TAI}}}. \tag{22}$$

Let κ denote the delay difference of two packets from entrance of the JCS to the theoretical eligibility time of the RCSP in TAI, i.e.,

$$\kappa^{\mathcal{H}_{\mathrm{TAI}}} \triangleq \left(\tilde{E}_1^{\mathcal{H}_{\mathrm{TAI}}} - A_1^{\mathcal{H}_{\mathrm{TAI}}}\right) - \left(\tilde{E}_2^{\mathcal{H}_{\mathrm{TAI}}} - A_2^{\mathcal{H}_{\mathrm{TAI}}}\right). \tag{23}$$

$|\kappa^{\mathcal{H}_{\mathrm{TAI}}}|$ is less than the jitter bound of Theorem 1 when $\Delta^{\mathrm{L}} = \Delta^{\mathrm{U}} = 0$; $|\kappa^{\mathcal{H}_{\mathrm{TAI}}}| \leq V^0 = \overline{\psi} + \underline{\psi} + 2\epsilon$. Then by (22), we have:

$$\tilde{E}_1^{\mathcal{H}_{\mathrm{TAI}}} - \tilde{E}_2^{\mathcal{H}_{\mathrm{TAI}}} = \tau^{\mathcal{H}_{\mathrm{TAI}}} + \kappa^{\mathcal{H}_{\mathrm{TAI}}}, \tag{24}$$

which shows the interspacing between the theoretical eligibility times of two packets at the RCSP in TAI. Observing this interspacing with $\mathcal{H}_2$, we obtain

$$\tilde{E}_1^{\mathcal{H}_2} - \tilde{E}_2^{\mathcal{H}_2} = \tau^{\mathcal{H}_{\mathrm{TAI}}} + \kappa^{\mathcal{H}_{\mathrm{TAI}}} + \gamma, \tag{25}$$

where γ is the difference in the measurement of the interspacing between $\mathcal{H}_{\mathrm{TAI}}$ and $\mathcal{H}_2$, bounded by (1). The actual eligibility times of the packets from RCSP are obtained by getting the floor of the theoretical eligibility times divided by Δ (Section IV). Hence, if $\tau^{\mathcal{H}_{\mathrm{TAI}}} + \kappa^{\mathcal{H}_{\mathrm{TAI}}} + \gamma < \Delta^{\mathrm{L}}$, the two packets may have the same actual eligibility times (leave RCSP back-to-back). The probability of this phenomenon is

$$\mathbb{P}\left[\text{backToBack}\right] = 1 - \frac{\tau^{\mathcal{H}_{\mathrm{TAI}}} + \kappa^{\mathcal{H}_{\mathrm{TAI}}} + \gamma}{\Delta^{\mathrm{L}}} \approx 1 - \frac{\tau^{\mathcal{H}_{\mathrm{TAI}}}}{\Delta^{\mathrm{L}}},$$

which implies that, the smaller the interspacing of the two packets when entering the JCS, the larger is the probability of having the two packets with the same actual eligibility time and leave the RSCP back-to-back. When two packets are back-to-back from one RCSP, then similar to scenario 1, there is 50% chance of reordering for the two packets at the output of the next downstream RCSP. Due to the independence of the two events (being back-to-back at the output of the RCSP and reordering at next downstream RCSP), the chance of reordering is $0.5\left(1 - \tau^{\mathcal{H}_{\mathrm{TAI}}}/\Delta^{\mathrm{L}}\right)$.

One approach to tackle the reordering issue of dampers with tolerance is to place re-sequencing buffers after the dampers

to correct the reordering that they cause. With this approach, it is crucial to find proper time-out value and size for the re-sequencing buffers. As shown in [18], two reordering metrics, namely reordering late-time offset (RTO) and reordering byte offset (RBO) respectively give the time-out value and size of a re-sequencing buffer. We obtain these metrics for dampers as a direct result of [18]:

Corollary 2. *Consider Fig. 4 and a flow that has arrival curve $\alpha^{\mathcal{H}_{\mathrm{TAI}}}$ at the entrance of the block. Then, the RTO for the flow from the entrance of the block to the output of the damper with tolerance, measured in TAI, is λ^{TAI} and the corresponding RBO is ζ:*

$$\lambda^{\mathrm{TAI}} = \left[V - \left(\alpha^{\mathcal{H}_{\mathrm{TAI}}}\right)^{\downarrow}\left(2L^{\min}\right)\right]^{+}, \tag{26}$$

$$\zeta = \alpha^{\mathcal{H}_{\mathrm{TAI}}}(V) - L^{\min}, \tag{27}$$

where V is the jitter bound of the block, computed in Theorem 1, and $L^{\min}$ is the minimum packet length of the flow.

Example. Consider Example 1 of Section III-A with the same assumptions made after Theorem 1. Suppose that a flow has leaky-bucket arrival curve with rate 16 Mbps, in TAI, burstiness 10 KBytes at source and minimum packet length 100 Bytes. We computed that the jitter bound is 1.262 μs from the source to the output of the first damper. Then the RTO (time-out value) is 1.262 μs and the RBO (required buffer size) is 10003 Bytes.

Another approach to tackle reordering is to use dampers with FIFO constraint, as discussed in Section IV and analyzed in the next section.

VII. Analysis of Dampers with FIFO constraints

As mentioned earlier, one way to avoid packet reordering within dampers with tolerance is to replace them with dampers with FIFO constraint, namely, re-sequencing and HoL dampers. The goal of this section is to provide delay and jitter bounds when dampers with FIFO constraint are used. In this context, "FIFO" and "re-sequencing" are with respect to the aggregate of all packets that use a damper of interest. When all the BDSs and JCSs within a flow path are FIFO, using re-sequencing or HoL dampers, in contrary to dampers with tolerances, can provide end-to-end in-order packet delivery. However, this might impact the delay and jitter bounds computed in Theorem 1. To this end, we capture the impact of using re-sequencing or HoL dampers instead of dampers with tolerances in terms of delay and jitter bounds in Theorem 3 and Theorem 4 when all systems are FIFO. Then, we see in Theorem 5 and Theorem 6 that the presence of a non-FIFO system (BDS or JCS) in the flow path considerably worsens the delay and jitter bounds obtained when all systems are FIFO. This phenomenon does not occur with dampers without FIFO constraint because the results in Section V hold whether the JCSs and BDSs are FIFO or not.

Theorem 3. *Consider the block of systems in Fig. 8 where all the JCSs and BDSs are FIFO and the damper is an instance of re-sequencing dampers with tolerances $\left(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}}\right)$. Assume that the clocks follow the description in Section III-B. Then, the delay and jitter bounds of the block, in TAI, is the same as the bounds in Theorem 1.*

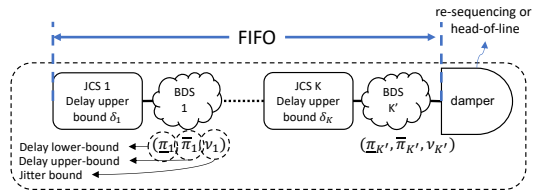

Fig. 8: The notations used in Theorem 3 and Theorem 4.

The proof is in Appendix A-D. It consists in two steps. First, we use an abstraction of a re-sequencing damper with tolerances $\left(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}}\right)$ as a damper with tolerances $\left(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}}\right)$ followed by a re-sequencing buffer that preserve the order of packet at their entrance to the damper with tolerances. Second, by the re-sequencing-for-free property of the re-sequencing buffers [18], we obtain the bounds.

Remark. We have seen in the previous section that even if all BDSs and JCSs are FIFO in a flow path, dampers with tolerance may cause packet reordering due to the tolerances, non-ideal clocks and errors in packet header computation. Theorem 3 indicates that in such a case, placing a re-sequencing damper avoids packet reordering with the same delay and jitter bounds as if dampers with tolerances are used.

Theorem 4. *Consider the block of systems in Fig. 8 where all the JCSs and BDSs are FIFO and the damper is an instance of head-of-line dampers with tolerances ($\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}}$) and processing-time bounds ($\phi^{\min}, \phi^{\max}$). Assume that the clocks follow the description in Section III-B. Then if $\phi^{\max} = 0$, the delay and jitter bounds are the same as the bounds in Theorem 1. Otherwise, for a flow with per-packet arrival curve α at the entrance of the block,*

1) *the delay upper-bound is increased by θ,*
2) *the delay lower-bound is increased by $\phi^{\min}$,*
3) *the jitter bound is increased by $\theta - \phi^{\min}$,*

where θ is a delay upper-bound of a single-server FIFO queue with maximum processing time of $\phi^{\max}$, computed as

$$\theta = \max_{k \in \mathbb{N}} \left\{ k\phi^{\max} - \alpha^{\downarrow}(k) + V \right\}, \tag{28}$$

where V is the jitter bound computed in Theorem 1 and

$$\alpha^{\downarrow}(k) = \inf\left\{t \geq 0 | \alpha(t) \geq k\right\}.$$

The proof is in Appendix A-E. The proof consists in two steps. First, we prove that an HoL damper is equivalent to re-sequencing damper with tolerances ($\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}}$) followed by a single-server FIFO queue with service times within ($\phi^{\min}, \phi^{\max}$). Second, using the bounds of Theorem 3 and obtaining delay and jitter bounds on the single-server queue, the theorem is proven.

Remark. HoL dampers, in contrary to re-sequencing dampers, imposes some queuing delay, captured by θ in (28). The queuing delay is maximized for the last packet of a packet sequence when all become eligible at the same time; then since the HoL damper examines only the packet at the head of the queue, the last packet of the sequence is delayed as much as the processing delay of all the preceding packets.

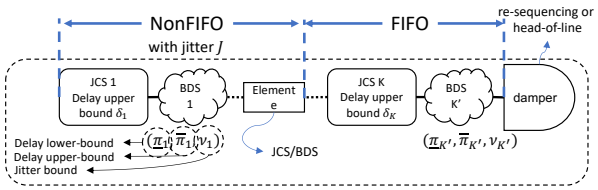

Fig. 9: The notations used in Theorem 5 and Theorem 6.

So far we provide delay and jitter bounds when all the systems are FIFO; however, the FIFO condition might not be always met for all systems such as multi-stage switching fabrics, multi-path routing of packets or packet duplication [40]–[42]. Hence, in the following theorems we capture the impact of non-FIFO behavior of systems on the delay and jitter bounds when re-sequencing and HoL dampers are used.

Theorem 5. *Consider Fig. 9 where system e (a BDS or a JCS) is the last non-FIFO system in the block and the damper is an instance of re-sequencing damper. Let us call J as the jitter from JCS 1 to system e (included), in TAI. Then, the delay upper-bound and jitter bound of the block, in TAI, are increased by J comparing to the bounds in Theorem 3.*

The bounds are tight, i.e., for any packet that experiences the delay equal to $\overline{D}$, there is system and an execution trace that another packet experiences a delay equal to $\overline{D} + J$.

The proof is in Appendix A-F. The proof has two parts. First, we show that delay upper-bound is increased by J while the delay lower-bound remains unchanged. Second, we provide a scenario where two packets with interspacing J enter the block and leave the element e back-to-back while their order is changed. We show that when the second packet experiences a delay $\overline{D}$, the first packet experiences a delay of $\overline{D}+J$ and the second packet leaves the re-sequencing damper before the first packet.

Theorem 6. *Consider Fig. 9 where system e (a BDS or a JCS) is the last non-FIFO system in the block and the damper is an instance of HoL damper. Let us call J as the jitter from JCS 1 to system e (included), in TAI. Then, comparing to Theorem 4, the delay upper-bound and jitter bound of the block, in TAI, are increased by J if $\phi^{\max} = 0$, and are increased by $2J$ if $\phi^{\max} > 0$.*

The proof is in Appendix A-G. The proof consists in two steps. First, similarly to the proof of Theorem 3, we abstract an HoL damper as a re-sequencing damper followed by a single-server FIFO queue. Second, by summing the bounds obtained in Theorem 5 and the bounds on the FIFO queue, the statement is proven. In the case $\phi^{\max} > 0$, the bounds are increased once by J within the re-sequencing damper and once within the FIFO queue as a result of propagated arrival curve at the output of the re-sequencing damper.

Remark. Similarly to Corollary 1, propagated arrival curve of a flow, with arrival curve $\alpha^{\mathcal{H}_{\text{TAI}}}(t)$ at the entrance of a block, is $\alpha^{\mathcal{H}_{\text{TAI}}}(t+\bar{V})$ at the output of re-sequencing or HoL damper, where $\bar{V}$ is the jitter of the block computed by applying the corresponding theorem.

Remark. Theorem 5 and Theorem 6 show that when there is a non-FIFO system in a block, placement of a damper with FIFO constraint is counterproductive. First, comparing to placement of dampers with tolerances, the jitter is increased; in result, it leads to an increase in the burstiness of the propagated arrival curve. Second, the damper with FIFO constraint preserves the wrong order of the packets, which occurred within the non-FIFO system.

VIII. Numerical Evaluation

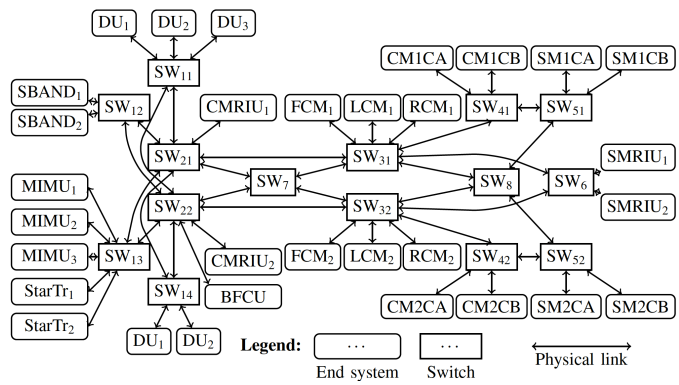

Fig. 10: The Orion crew exploration vehicle network.

We illustrate our theoretical results on the Orion crew exploration vehicle network, as described in [43] and depicted in Fig. 10, taken from [39]. For the delay and jitter analysis, we used Fixed-Point TFA [39], [44] as there are cyclic dependencies. The device clocks are not synchronized. The link rates are 1 Gbps. The output ports use a non-preemptive TSN scheduler with Credit-based Shapers (CBSs) with per-class FIFO queuing [45], [46]; from highest to lowest priority, the classes are CDT, A, B, and Best Effort (BE). The CBSs are used separately for classes A and B. The CBS parameters $idleslope$s are set to 50% and 25% of the link rate respectively for classes A and B [46]. In each switch, the switching fabric has a delay between 0.5 μs to 2 μs [47]. The CDT traffic has a leaky-bucket arrival curve with rate 6.4 kilobytes per second and burst 64 bytes. The maximum packet length of classes B and BE is 1500 bytes. We focus on class A. Using the results in [45], a rate-latency service curve offered to class A is $\beta(t) = 62.49e6[t - t_0]^+$ bytes with $t_0 = 12.5$ μs.

Class A contains 40 flows with constant packet size 147 bytes, which transmit 10 packets every 8 ms. The flows traverse between 2 to 9 hops. We assume all switching fabrics and output queuing systems implement DHU unit and therefore are JCSs; the propagation delays are considered as BDSs with zero jitter. We examine the case where no damper is placed and the case where dampers are placed at every switch and the destinations. For the choice of dampers, we considered individually the full deployment of RCSP ($\Delta^{\text{L}} = 1$ μs, $\Delta^{\text{U}} = 2$ ns), RGCQ ($\Delta^{\text{L}} = 2$ ns, $\Delta^{\text{U}} = 1$ μs) with TE time-stamping, FOPLEQ ($\Delta^{\text{L}} = 1$ μs, $\Delta^{\text{U}} = 2$ ns) and a head-of-line damper ($\phi^{\min} = 0, \phi^{\max} = 5$ ns, $\Delta^{\text{L}} = \Delta^{\text{U}} = 2$ ns).

Fig. 11 shows the end-to-end jitter bounds of the flows for full deployment of RCSP and RGCQ with TE time-stamping. For each of the cases, the basic jitter computation

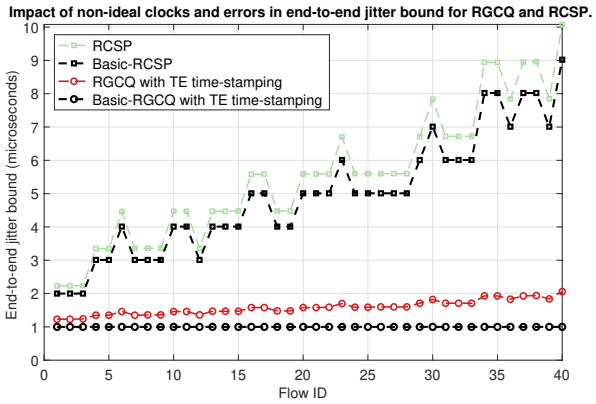

Fig. 11: The end-to-end jitter bounds for RCSP and RGCQ with TE time-stamping using basic jitter computation and using theorems 1 and 2.

only considers the jitter imposed by the tolerances of the dampers and ignore the impact of non-ideal clocks and errors in the computation of damper header. Fig. 11 also shows the true jitter bound for the case of RCSP, using Theorem 1, and for the case of RGCQ with TE time-stamping using Theorem 2. We see that non-ideal clocks and errors can increase jitter by 11% in the case of RCSP and 106% in the case of RGCQ with TE time-stamping. We also see that the TE time-stamping used with RGCQ can significantly reduce the end-to-end jitter comparing to the default time-stamping used with RCSP.

Fig. 12 shows the end-to-end delay and jitter bounds of the flows when no damper is used and when there is a full deployment as above. All switching fabrics are FIFO. We see that without damper, the delay upper-bound is smaller compared to full damper deployments; this is due to the line-shaping effect when computing the queuing delay bounds in the absence of dampers. However, as expected, the full deployment of dampers significantly reduces the jitter bounds. In this computation, the HoL damper provides quasi similar jitter bound as RGCQ with TE time-stamping and FOPLEQ gives the exact same jitter bound as RCSP as seen in Theorem 3.

Fig. 13 shows the end-to-end jitter bounds of the flows for FOPLEQ and HoL damper considering the switching fabrics are FIFO and are not FIFO. The figure shows that with FOPLEQ the jitter is significantly increased that is due to the jitter imposed by the output queuing, as seen in Theorem 5. It also shows that jitter bounds are worse in the case of HoL damper as discussed in Theorem 6.

IX. Conclusion

We have presented a theory to compute delay and jitter bounds in a network that implements dampers with non-ideal clocks. We have shown that dampers without FIFO constraint can cause packet reordering even if all network elements are FIFO; re-sequencing dampers and head-of-line dampers avoid the problem; the former come with no jitter or delay penalty, and the latter with a small, quantified penalty. However, when a flow path contains non-FIFO elements, re-sequencing dampers and head-of-line dampers do not perform well.

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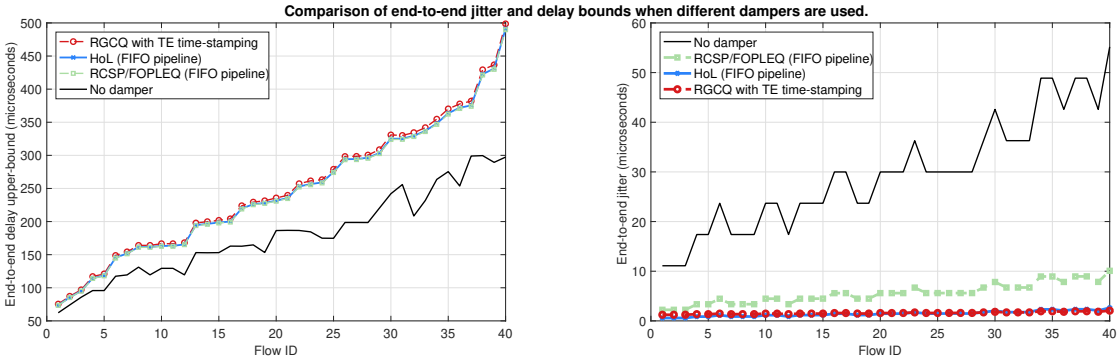

Fig. 12: The end-to-end delay bounds (left) and jitter bounds (right) for full deployment of dampers and in the absence of dampers. For FOPLEQ and head-of-line (HoL) dampers, we assume that all the elements are FIFO.

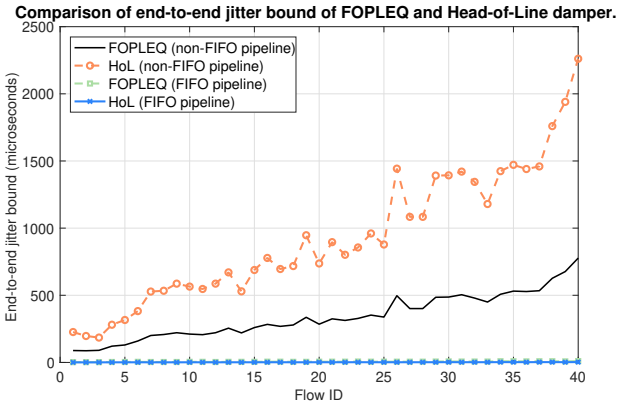

Fig. 13: The end-to-end jitter bounds for FOPLEQ and head-of-line dampers when switching fabrics are FIFO or not.

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Supplementary Material

Analysis of Dampers in Time-Sensitive Networks with Non-ideal Clocks

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Appendix A
Proofs

A. Lemmas for Section IV

Lemma 1. *Consider a non-decreasing sequence $I = \{I_1, \ldots, I_n\}$ and a sequence $\phi = \{\phi_1, \ldots, \phi_n\}$. Assume the sequence $O = \{O_1, \ldots, O_n\}$ is defined by*

$$O_1 = I_1 + \phi_1, \quad O_n = \max(I_n, O_{n-1}) + \phi_n.$$

Then a closed-form formula for O is:

$$O_n = \max_{m \le n} \left\{ I_m + \sum_{i=m}^{n} \phi_i \right\}.$$

Proof. We prove by induction. Base case $n = 1$.

$$O_1 = I_1 + \phi_1, \tag{29}$$

as required by the lemma.

Induction step. We assume that the lemma holds for all $i < n$. Then for $i = n - 1$, by the closed-form formula we have:

$$O_{n-1} = \max_{m \le n-1} \left\{ I_m + \sum_{i=m}^{n-1} \phi_i \right\}. \tag{30}$$

Then, using the recursive definition of O_n:

$$\begin{aligned} O_n &= \max(I_n, O_{n-1}) + \phi_n \\ &= \max\left(I_n + \phi_n, \max_{m \le n-1} \left\{ I_m + \sum_{i=m}^{n-1} \phi_i \right\} + \phi_n \right) \\ &= \max\left(I_n + \phi_n, \max_{m \le n-1} \left\{ I_m + \sum_{i=m}^{n} \phi_i \right\} \right) \\ &= \max_{m \le n} \left\{ I_m + \sum_{i=m}^{n} \phi_i \right\}. \end{aligned} \tag{31}$$

□

Lemma 2. *Let a, $x^{\min} \le x^{\max}$ and $y^{\min} \le y^{\max}$ be five fixed real numbers. For any $z \in \mathbb{R}$, if*

$$x^{\min} + \max(a, y^{\min}) \le z \le x^{\max} + \max(a, y^{\max}), \tag{32}$$

then there exists some $x, y \in \mathbb{R}$ such that

$$z = x + \max(a, y), \tag{33}$$

$$x \in [x^{\min}; x^{\max}], \tag{34}$$

$$y \in [y^{\min}; y^{\max}]. \tag{35}$$

Comversely, if there exists $x, y \in \mathbb{R}$ such that (33)–(35) *hold, then z satisfies* (32).

Proof. 1) Let $D = [x^{\min}; x^{\max}] \times [y^{\min}; y^{\max}]$ and f the mapping $D \to \mathbb{R}$ defined by $f(x, y) = x + \max(a, y)$. f is continuous and D is compact and connected, therefore $f(D)$ is compact and connected. The compact and connected subsets of $\mathbb{R}$ are the closed, bounded intervals, therefore $f(D) = [m; M]$ for some $m, M \in \mathbb{R}$. Necessarily, m is the minimum of f over D and M is the maximum of f over D.

Now for every $(x, y) \in D$:

$$f(x^{\min}, y^{\min}) \le f(x, y) \le f(x^{\max}, y^{\max}). \tag{36}$$

It follows that the minimum of f over D is $f(x^{\min}, y^{\min})$, i.e. $m = f(x^{\min}, y^{\min})$. Similarly, $M = f(x^{\max}, y^{\max})$. Now let $z \in \mathbb{R}$ that satisfies (32), i.e. $z \in [m; M] = f(D)$. Thus, there exists some $(x, y) \in D$ such that $z = f(x, y)$, i.e. there exists $x, y \in \mathbb{R}$ such that (33)–(35) hold.

2) Conversely, if there exists $x, y \in \mathbb{R}$ such that (33)–(35) hold, then $z = f(x, y)$ and thus $m \le z \le M$, i.e. (32) holds. □

B. Proof of Theorem 1

Let us define d_i as the delay of JCS i ($i = 1, \ldots, K$), π_j as the delay of BDS j ($j = 1, \ldots, K'$) and t as the delay of the damper. Assume that JCS i is operating with clock $\mathcal{H}_i$ and the damper is operating with clock $\mathcal{H}_{\text{damper}}$. Then, the delay of the block, in TAI, is:

$$\begin{aligned} d^{\mathcal{H}_{\text{TAI}}} &= \sum_{i=1}^{K} d_i^{\mathcal{H}_{\text{TAI}}} + \sum_{j=1}^{K'} \pi_j^{\mathcal{H}_{\text{TAI}}} + t^{\mathcal{H}_{\text{TAI}}} = \sum_{i=1}^{K} d_i^{\mathcal{H}_i} \\ &\quad + \sum_{j=1}^{K'} \pi_j^{\mathcal{H}_{\text{TAI}}} + t^{\mathcal{H}_{\text{damper}}} + \gamma, \end{aligned} \tag{37}$$

where $\gamma = \sum_{i=1}^{K} \left(d_i^{\mathcal{H}_{\text{TAI}}} - d_i^{\mathcal{H}_i} \right) + \left(t^{\mathcal{H}_{\text{TAI}}} - t^{\mathcal{H}_{\text{damper}}} \right)$. By (3) and (4), the delay of a packet with damper header H inside the damper is

$$H - \Delta^{\text{L}} \le t^{\mathcal{H}_{\text{damper}}} \le H + \Delta^{\text{U}}. \tag{38}$$

Moreover, the damper header is incremented when the packet is passing by a JCS. Therefore, by (12) and accounting for the errors in the computation of damper header, we have:

$$H = \sum_{i=1}^{K} (\delta_i - d_i^{\mathcal{H}_i} + e) = \sum_{i=1}^{K} \delta_i - \sum_{i=1}^{K} d_i^{\mathcal{H}_i} + Ke, \tag{39}$$

where e is defined in Section IV-C2. Using (39) and the upper bound in (38), (37) gives:

$$\begin{aligned} d^{\mathcal{H}_{\text{TAI}}} &\le \sum_{i=1}^{K} d_i^{\mathcal{H}_i} + \sum_{j=1}^{K'} \pi_j^{\mathcal{H}_{\text{TAI}}} + \left(\sum_{i=1}^{K} \delta_i - \sum_{i=1}^{K} d_i^{\mathcal{H}_i} + Ke \right) \\ &\quad + \Delta^{\text{U}} + \gamma = \sum_{i=1}^{K} \delta_i + \sum_{j=1}^{K'} \pi_j^{\mathcal{H}_{\text{TAI}}} + \Delta^{\text{U}} + Ke + \gamma. \end{aligned} \tag{40}$$

By Lemma 3, $\gamma \le \overline{\psi}$; also $|e| \le \epsilon$; furthermore, the delay of the packet inside the BDS j is less than its worst-case delay, i.e., $\pi_{j,\text{worst}}^{\mathcal{H}_{\text{TAI}}}$. Therefore:

$$d^{\mathcal{H}_{\text{TAI}}} \le \sum_{i=1}^{K} \delta_i + \sum_{j=1}^{K'} \pi_{j,\text{worst}}^{\mathcal{H}_{\text{TAI}}} + \Delta^{\text{U}} + K\epsilon + \overline{\psi}.$$

Similarly, using the lower bound in (38) and the value of H in (39), we have:

$$d^{\mathcal{H}_{\rm TAI}} \geq \sum_{i=1}^{K} d_i^{\mathcal{H}_i} + \sum_{j=1}^{K'} \pi_j^{\mathcal{H}_{\rm TAI}} + \left(\sum_{i=1}^{K} \delta_i - \sum_{i=1}^{K} d_i^{\mathcal{H}_i} + Ke\right) - \Delta^{\rm L} + \gamma = \sum_{i=1}^{K} \delta_i + \sum_{j=1}^{K'} \pi_j^{\mathcal{H}_{\rm TAI}} - \Delta^{\rm L} + Ke + \gamma. \tag{41}$$

By Lemma 3, $\gamma \geq -\underline{\psi}$; also, $|e| \leq \epsilon$; furthermore, the delay of the packet inside the BDS j is less than its best-case delay, i.e., $\pi_{j,\rm best}^{\mathcal{H}_{\rm TAI}}$. Therefore:

$$d^{\mathcal{H}_{\rm TAI}} \geq \sum_{i=1}^{K} \delta_i + \sum_{j=1}^{K'} \pi_{j,\rm best}^{\mathcal{H}_{\rm TAI}} - \Delta^{\rm L} - K\epsilon - \underline{\psi}_i.$$

By subtracting the lower and upper bounds in (41) and (42), we obtain a jitter bound for the block:

$$V = \sum_{j=1}^{K'} \left(\pi_{j,\rm worst}^{\mathcal{H}_{\rm TAI}} - \pi_{j,\rm best}^{\mathcal{H}_{\rm TAI}}\right) + \Delta^{\rm U} + \Delta^{\rm L} + 2K\epsilon + \overline{\psi} + \underline{\psi} = \sum_{j=1}^{K'} \nu_j^{\mathcal{H}_{\rm TAI}} + \Delta^{\rm U} + \Delta^{\rm L} + 2K\epsilon + \overline{\psi} + \underline{\psi}, \tag{42}$$

which proves the jitter bound. Note that $\pi_{j,\rm worst}^{\mathcal{H}_{\rm TAI}} - \pi_{j,\rm best}^{\mathcal{H}_{\rm TAI}} \leq \nu_j^{\mathcal{H}_{\rm TAI}}$.
Moreover, since $\pi_{j,\rm worst}^{\mathcal{H}_{\rm TAI}} \leq \overline{\pi}_j^{\mathcal{H}_{\rm TAI}}$ and $\pi_{j,\rm best}^{\mathcal{H}_{\rm TAI}} \geq \underline{\pi}_j^{\mathcal{H}_{\rm TAI}}$, we have:

$$d^{\mathcal{H}_{\rm TAI}} \leq \sum_{i=1}^{K} \delta_i + \sum_{j=1}^{K'} \overline{\pi}_j^{\mathcal{H}_{\rm TAI}} + \Delta^{\rm U} + K\epsilon + \overline{\psi} = \overline{D},$$
$$d^{\mathcal{H}_{\rm TAI}} \geq \sum_{i=1}^{K} \delta_i + \sum_{j=1}^{K'} \pi_j^{\mathcal{H}_{\rm TAI}} - \Delta^{\rm L} - K\epsilon - \underline{\psi} = \underline{D}. \tag{43}$$

Proof of tightness. Consider a packet that enters JCS 1. We show scenarios where the packet reaches the delay bound in the statement of the theorem; since $\overline{\psi}$ can take different values due to the $\min(.)$ function, we give two different scenarios.

First scenario. Assume that the clocks $\mathcal{H}_i$, $i = 1, ..., K$, and $\mathcal{H}_{\rm damper}$ are adversarial and faster than TAI such that for any delay measurement d we have:

$$d^{\mathcal{H}_{\rm TAI}} = \rho d^{\mathcal{H}_i} + \eta, \quad i = 1, ..., K$$
$$d^{\mathcal{H}_{\rm TAI}} = \rho d^{\mathcal{H}_{\rm damper}} + \eta. \tag{44}$$

This scenario assumes that for any clock $\mathcal{H}_i$, $\rho d^{\mathcal{H}_i} + \eta \leq d^{\mathcal{H}_i} + 2\omega$ and $\rho d^{\mathcal{H}_{\rm damper}} + \eta \leq d^{\mathcal{H}_{\rm damper}} + 2\omega$.

Let us define H_i as the damper header that is computed in JCS i. Then, let the packet experience a delay $d_i^{\mathcal{H}_i} \leq \delta_i$ in JCS i in its local time; then the damper header written for this packet is

$$H_1 = \delta_1 - d_1^{\mathcal{H}_1} + \epsilon,$$
$$H_i = H_{i-1} + \delta_i - d_i^{\mathcal{H}_i} + \epsilon, \quad i = 2, ..., K$$

assuming adversarial condition in the damper header computation error. The packet experiences a delay equal to $\overline{\pi}_j^{\mathcal{H}_{\rm TAI}}$ in BDS j. Finally, the damper computes the eligibility time and releases it at the latest; i.e., the packet experiences a delay

$$t^{\mathcal{H}_{\rm damper}} = H_K + \Delta^{\rm U} = \sum_{u=1}^{K} \delta_u - \sum_{u=1}^{K} d_u^{\mathcal{H}_u} + K\epsilon + \Delta^{\rm U}.$$

Therefore, for the damper, the delay of the packet in TAI, using (44), is:

$$t^{\mathcal{H}_{\rm TAI}} = \rho \left(\sum_{u=1}^{K} \delta_u - \sum_{u=1}^{K} d_u^{\mathcal{H}_u} + K\epsilon + \Delta^{\rm U}\right) + \eta. \tag{45}$$

Also, for JCS i, the delay of the packet in TAI is:

$$d_i^{\mathcal{H}_{\rm TAI}} = \rho d_i^{\mathcal{H}_i} + \eta. \tag{46}$$

Now, to compute the per-hop delay of the packet, we sum up all the delays in TAI:

$$\begin{aligned} d_{\rm hop}^{\mathcal{H}_{\rm TAI}} &= \sum_{u=1}^{K} d_u^{\mathcal{H}_{\rm TAI}} + \sum_{j=1}^{K'} \overline{\pi}_j^{\mathcal{H}_{\rm TAI}} + t^{\mathcal{H}_{\rm TAI}} = \sum_{u=1}^{K} \left(\rho d_u^{\mathcal{H}_i} + \eta\right) \\ &+ \sum_{j=1}^{K'} \overline{\pi}_j^{\mathcal{H}_{\rm TAI}} + \rho \left(\sum_{u=1}^{K} \delta_u - \sum_{u=1}^{K} d_u^{\mathcal{H}_u} + K\epsilon + \Delta^{\rm U}\right) + \eta \\ &= \rho(\sum_{u=1}^{K} \delta_u + K\epsilon + \Delta^{\rm U}) + \sum_{j=1}^{K'} \overline{\pi}_j^{\mathcal{H}_{\rm TAI}} + (K+1)\eta \\ &= \sum_{u=1}^{K} \delta_u + \sum_{j=1}^{K'} \overline{\pi}_j^{\mathcal{H}_{\rm TAI}} + \Delta^{\rm U} + K\epsilon + \overline{\psi}, \end{aligned} \tag{47}$$

which is equal to the delay bound in the statement of the theorem.

Second scenario. Assume that the clocks $\mathcal{H}_i$, $i = 1, ..., K$, and $\mathcal{H}_{\rm damper}$ are adversarial and faster than TAI such that for any delay measurement d we have:

$$d^{\mathcal{H}_{\rm TAI}} = d^{\mathcal{H}_i} + 2\omega, \quad i = 1, ..., K$$
$$d^{\mathcal{H}_{\rm TAI}} = d^{\mathcal{H}_{\rm damper}} + 2\omega. \tag{48}$$

This scenario assumes that for any clock $\mathcal{H}_i$, $\rho d^{\mathcal{H}_i} + \eta \geq d^{\mathcal{H}_i} + 2\omega$ and $\rho d^{\mathcal{H}_{\rm damper}} + \eta \geq d^{\mathcal{H}_{\rm damper}} + 2\omega$. Then following the same steps as the previous scenario, we have:

$$t^{\mathcal{H}_{\rm TAI}} = \sum_{u=1}^{K} \delta_u - \sum_{u=1}^{K} d_u^{\mathcal{H}_u} + K\epsilon + \Delta^{\rm U} + 2\omega,$$
$$d_i^{\mathcal{H}_{\rm TAI}} = d_i^{\mathcal{H}_i} + 2\omega, \quad \forall i \in \{1, \ldots, K\}. \tag{49}$$

This gives:

$$\begin{aligned} d_{\rm hop}^{\mathcal{H}_{\rm TAI}} &= \sum_{u=1}^{K} d_u^{\mathcal{H}_{\rm TAI}} + \sum_{j=1}^{K'} \overline{\pi}_j^{\mathcal{H}_{\rm TAI}} + t^{\mathcal{H}_{\rm TAI}} = \sum_{u=1}^{K} \left(d_u^{\mathcal{H}_i} + 2\omega\right) \\ &+ \sum_{j=1}^{K'} \overline{\pi}_j^{\mathcal{H}_{\rm TAI}} + \sum_{u=1}^{K} \delta_u - \sum_{u=1}^{K} d_u^{\mathcal{H}_u} + K\epsilon + \Delta^{\rm U} + 2\omega \\ &= \sum_{u=1}^{K} \delta_u + K\epsilon + \Delta^{\rm U} + \sum_{j=1}^{K'} \overline{\pi}_j^{\mathcal{H}_{\rm TAI}} + 2(K+1)\omega \\ &= \sum_{u=1}^{K} \delta_u + \sum_{j=1}^{K'} \overline{\pi}_j^{\mathcal{H}_{\rm TAI}} + \Delta^{\rm U} + K\epsilon + \overline{\psi}, \end{aligned} \tag{50}$$

which is equal to the delay bound in the statement of the theorem. The tightness for delay lower bound happens when the clocks $\mathcal{H}_i$, $i = 1, ..., K$, and $\mathcal{H}_{\text{damper}}$ are adversarial and slower than TAI. Similarly to the tightness proof of delay upper-bound, two tightness scenarios are given for the two possible values of $\underline{\psi}$. For the first scenario, for any delay measurement d, we have:

$$d^{\mathcal{H}_{\text{TAI}}} = \frac{1}{\rho}\left(d^{\mathcal{H}_i} - \eta\right), \quad i = 1, ..., K,$$
$$d^{\mathcal{H}_{\text{TAI}}} = \frac{1}{\rho}\left(d^{\mathcal{H}_{\text{damper}}} - \eta\right), \tag{51}$$

and for the second scenario, we have:

$$d^{\mathcal{H}_{\text{TAI}}} = d^{\mathcal{H}_i} - 2\omega, \quad i = 1, ..., K,$$
$$d^{\mathcal{H}_{\text{TAI}}} = d^{\mathcal{H}_{\text{damper}}} - 2\omega. \tag{52}$$

Considering the damper releases the packets at the earliest, the rest of the proof follows the same steps as the tightness proof of delay upper-bound.

Lemma 3. *$-\underline{\psi} \leq \gamma \leq \overline{\psi}$, where $\underline{\psi}$ and $\overline{\psi}$ are defined in* (14)*:*

Proof. By definition of γ, we have:

$$\gamma = \sum_{j=1}^{K}\left(d_j^{\mathcal{H}_{\text{TAI}}} - d_j^{\mathcal{H}_j}\right) + \left(t^{\mathcal{H}_{\text{TAI}}} - t^{\mathcal{H}_{\text{damper}}}\right). \tag{53}$$

First we prove the upper bound. By (1) the following holds for any JCS j:

$$d_j^{\mathcal{H}_{\text{TAI}}} - d_j^{\mathcal{H}_j} \leq (\rho - 1)d_j^{\mathcal{H}_j} + \eta,$$
$$d_j^{\mathcal{H}_{\text{TAI}}} - d_j^{\mathcal{H}_j} \leq 2\omega. \tag{54}$$

Using the value of H in (39) and the upper bound in (38), we have $t^{\mathcal{H}_{\text{damper}}} \leq \sum_{j=1}^{K}\left(\delta_j - d_j^{\mathcal{H}_j} + \epsilon\right) + \Delta^{\text{U}}$. Hence, similarly to the previous equation:

$$t^{\mathcal{H}_{\text{TAI}}} - t^{\mathcal{H}_{\text{damper}}} \leq (\rho - 1)\Big(\Delta^{\text{U}} + \sum_{j=1}^{K}\left(\delta_j - d_j^{\mathcal{H}_j} + \epsilon\right)\Big) + \eta,$$
$$t^{\mathcal{H}_{\text{TAI}}} - t^{\mathcal{H}_{\text{damper}}} \leq 2\omega. \tag{55}$$

We first consider the case that the synchronization inequality is dominating for all systems (i.e., the second line of (54) and (55)). Hence, we have:

$$\gamma \leq \sum_{j=1}^{K} 2\omega + 2\omega = 2(K+1)\omega. \tag{56}$$

Second, we consider the case that the free-running mode is dominating for all systems (i.e., in the first line of (54) and (55)). Then, we have:

$$\begin{aligned}\gamma \leq & \sum_{j=1}^{K}\left((\rho-1)d_j^{\mathcal{H}_j} + \eta\right) + (\rho-1)\Delta^{\text{U}} \\ & + (\rho-1)\left(\sum_{j=1}^{K}\left(\delta_j - d_j^{\mathcal{H}_j} + \epsilon\right)\right) + \eta \\ = & (\rho-1)\left(\Delta^{\text{U}} + \sum_{j=1}^{K}(\delta_j + \epsilon)\right) + (K+1)\eta.\end{aligned} \tag{57}$$

Finally, by (56) and (57), $\gamma \leq \overline{\psi}$.

Next, we prove the lower bound. Similarly, by (1) the following holds for any JCS j:

$$d_j^{\mathcal{H}_{\text{TAI}}} - d_j^{\mathcal{H}_j} \geq -\left(1 - \frac{1}{\rho}\right)d_j^{\mathcal{H}_j} - \frac{\eta}{\rho},$$
$$d_j^{\mathcal{H}_{\text{TAI}}} - d_j^{\mathcal{H}_j} \geq -2\omega. \tag{58}$$

Using the value of H in (39) and the upper bound in (38), we have $t^{\mathcal{H}_{\text{damper}}} \geq \sum_{j=1}^{K}\left(\delta_j - d_j^{\mathcal{H}_j} - \epsilon\right) - \Delta^{\text{L}}$. Hence:

$$t^{\mathcal{H}_{\text{TAI}}} - t^{\mathcal{H}_{\text{damper}}} \geq -(1 - \frac{1}{\rho})(-\Delta^{\text{L}} + \sum_{j=1}^{K}(\delta_j - d_j^{\mathcal{H}_j} - \epsilon)) - \frac{\eta}{\rho},$$
$$t^{\mathcal{H}_{\text{TAI}}} - t^{\mathcal{H}_{\text{damper}}} \geq -2\omega. \tag{59}$$

We first consider the case that the synchronization inequality is dominating for all systems (i.e., the second line of (54) and (55)). Hence, we have:

$$\gamma \geq -\sum_{j=1}^{K} 2\omega - 2\omega = -2(K+1)\omega. \tag{60}$$

Second, we consider the case that the free-running mode is dominating for all systems (i.e., in the first line of (54) and (55)). Then, we have:

$$\begin{aligned}\gamma \geq & -\left(1 - \frac{1}{\rho}\right)\sum_{j=1}^{K} d_j^{\mathcal{H}_j} - \frac{K\eta}{\rho} \\ & - \left(1 - \frac{1}{\rho}\right)\left(-\Delta^{\text{L}} + \sum_{j=1}^{K}\left(\delta_j - d_j^{\mathcal{H}_j} - \epsilon\right)\right) - \frac{\eta}{\rho} \\ = & -\left(1 - \frac{1}{\rho}\right)\left(-\Delta^{\text{L}} + \sum_{j=1}^{K}(\delta_j - \epsilon)\right) - \frac{(K+1)\eta}{\rho}.\end{aligned} \tag{61}$$

Finally, by (60) and (61), $\gamma \geq -\underline{\psi}$. □

C. Proof of Theorem 2

Consider a packet that enters block 1 at time A. Let us denote the theoretical and actual eligibility time of the packet from the damper of block i as $\tilde{E}_i$ and E_i respectively. Then, the delay from A to the output of block N, i.e., E_N, is:

$$d_{\text{e2e}}^{\mathcal{H}_{\text{TAI}}} = E_N^{\mathcal{H}_{\text{TAI}}} - A^{\mathcal{H}_{\text{TAI}}} = \left(\tilde{E}_1^{\mathcal{H}_{\text{TAI}}} - A^{\mathcal{H}_{\text{TAI}}}\right) + \sum_{i=2}^{N-1}\left(\tilde{E}_i^{\mathcal{H}_{\text{TAI}}} - \tilde{E}_{i-1}^{\mathcal{H}_{\text{TAI}}}\right) + \left(E_N^{\mathcal{H}_{\text{TAI}}} - \tilde{E}_{N-1}^{\mathcal{H}_{\text{TAI}}}\right). \tag{62}$$

By Theorem 1 and setting the tolerances to zero, we can find delay and jitter bounds for $\left(\tilde{E}_1^{\mathcal{H}_{\text{TAI}}} - A^{\mathcal{H}_{\text{TAI}}}\right)$ in TAI. For any term $\left(\tilde{E}_i^{\mathcal{H}_{\text{TAI}}} - \tilde{E}_{i-1}^{\mathcal{H}_{\text{TAI}}}\right)$ in the summation, using Lemma 4, we can obtain delay and jitter bound by setting $\Delta_i^{\text{L}} = \Delta_i^{\text{U}} = 0$ (since we are interested to find the delay to the theoretical eligibility time at the damper i). Finally, we can apply again Lemma 4 to get the bounds for $\left(E_N^{\mathcal{H}_{\text{TAI}}} - \tilde{E}_{N-1}^{\mathcal{H}_{\text{TAI}}}\right)$. By

summing up the delay and jitter bounds of each term in (62), we get the bounds in the statement of the theorem.

Lemma 4. *Consider a block i in Fig. 5 that has K_i JCSs. Assume that TE time-stamping is used to compute damper headers. Let δ_{blk_i} denote the sum of the delay bounds of the JCSs in the block, $\underline{\pi}^{\mathcal{H}_{\mathrm{TAI}}}_{\mathrm{blk}_i}, \overline{\pi}^{\mathcal{H}_{\mathrm{TAI}}}_{\mathrm{blk}_i}$ and $\nu^{\mathcal{H}_{\mathrm{TAI}}}_{\mathrm{blk}_i}$ respectively denote the sum of delay lower and upper bounds and jitter bound of the BDSs. Then, the delay of a packet from theoretical eligibility time of damper $i-1$, $i = 2, \ldots, N$, to the actual eligibility time of damper i, in TAI, is upper-bounded by $\overline{D}_i$, low-bounded by $\underline{D}_i$ and has jitter bound V_i:*

$$\begin{aligned}
\overline{D}_i &= \delta_{\mathrm{blk}_i} + \overline{\pi}^{\mathcal{H}_{\mathrm{TAI}}}_{\mathrm{blk}_i} + \Delta^{\mathrm{U}}_{i-1} + \Delta^{\mathrm{U}}_i + K_i\epsilon + \overline{\psi}'_i,\\
\underline{D}_i &= \delta_{\mathrm{blk}_i} + \underline{\pi}^{\mathcal{H}_{\mathrm{TAI}}}_{\mathrm{blk}_i} + \Delta^{\mathrm{U}}_{i-1} - \Delta^{\mathrm{L}}_i - K_i\epsilon - \underline{\psi}'_i,\\
V_i &= \nu^{\mathcal{H}_{\mathrm{TAI}}}_{\mathrm{blk}_i} + \Delta^{\mathrm{U}}_i + \Delta^{\mathrm{L}}_i + 2K_i\epsilon + \overline{\psi}_i + \underline{\psi}'_i,
\end{aligned}$$

where,

$$\begin{aligned}
\overline{\psi}'_i &= \min\Big((\rho-1)\left(\delta_{\mathrm{blk}_i} + \Delta^{\mathrm{U}}_{i-1} + \Delta^{\mathrm{U}}_i + K_i\epsilon\right) + (K_i+1)\eta\\
&\quad, 2(K_i+1)\omega\Big),\\
\underline{\psi}'_i &= \min\Bigg(\left(1-\frac{1}{\rho}\right)\left(\delta_{\mathrm{blk}_i} + \Delta^{\mathrm{U}}_{i-1} - \Delta^{\mathrm{L}}_i - K_i\epsilon\right)\\
&\quad + \frac{(K_i+1)\eta}{\rho}, 2(K_i+1)\omega\Bigg).
\end{aligned} \tag{63}$$

Proof. The proof follows the same as Theorem 1 and using:

$$\begin{aligned}
H &= (\delta_1 + \Delta^{\mathrm{U}}_{i-1} - d^{\mathcal{H}_1}_1 + e) + \sum_{j=2}^{K}(\delta_j - d^{\mathcal{H}_j}_j + e)\\
&= \sum_{j=1}^{K}\delta_j - \sum_{i=1}^{K} d^{\mathcal{H}_i}_i + \Delta^{\mathrm{U}}_{i-1} + Ke,
\end{aligned} \tag{64}$$

instead of (39) for damper header computation. Note that here $d^{\mathcal{H}_j}_j$ is the delay from of the packet from start of time stamping at JCS j to its departure time. □

D. Proof of Theorem 3

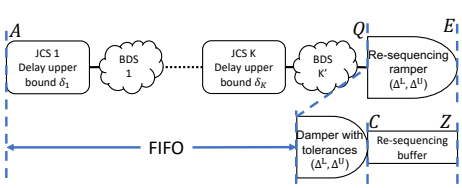

Fig. 14: The notations used in the proof of Theorem 3.

Consider Fig. 14 where A is the sequence of packet arrival times at entrance of the block, Q is the sequence of arrivals to the re-sequencing damper, and E is the sequence of actual eligibility times at the re-sequencing damper. By definition, the re-sequencing damper behaves as a damper with tolerances $(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}})$ followed by a re-sequencing buffer. Denote with C the actual eligibility times from the damper with tolerance and with Z the output times of the re-sequencing buffer; the equivalence means that $E = Z$.

By Theorem 1, the delay from A to C has lower bound $\underline{D}$, upper bound $\overline{D}$ and the jitter bound is V. Now, let $\mathcal{P}$ and $\mathcal{P}'$ be the sets of packets seen respectively at A and Q, i.e., $\mathcal{P}' \subseteq \mathcal{P}$; by defining $\mathcal{P}'$, we only include the packets of $\mathcal{P}$ that arrive to Q; therefore, by [18, Theorem 4], the re-sequencing buffer does not increase the worst-case delay and jitter from A to C. Hence, the delay and jitter bounds from A to Z are the same as from A to C, which proves the theorem.

E. Proof of Theorem 4

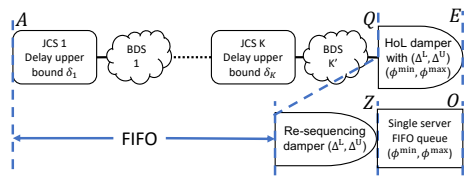

Fig. 15: The notations used in the proof of Theorem 4.

Consider Fig. 15 where A is the sequence of packet arrival times at JCS 1 (entrance of the block), Q is the sequence of arrivals to the head-of-line damper, $\tilde{E}$ and E are the sequences of theoretical and actual eligibility times at the head-of-line damper. By Lemma 5, the head-of-line damper is equivalent to a re-sequencing damper followed by a single-server FIFO queue with service time in range $[\phi^{\min}, \phi^{\max}]$. Denote with Z the output times of the re-sequencing damper and O as the output of the single-server FIFO queue; the equivalence means that $E = O$.

By Theorem 3, the delay from A to Z has lower bound $\underline{D}$, upper bound $\overline{D}$ and the jitter bound is V. Also, similarly to Corollary 1, arrival curve at Z is $\alpha_{\mathrm{reseq}}(t) = \alpha(t+V)$.

By Lemma 6, the delay upper-bound of the single-server FIFO queue is $\max_{k\in\mathbb{N}}\left\{k\phi^{\max} - \alpha^{\downarrow}_{\mathrm{reseq}}(k)\right\}$ for nonzero processing time, i.e. $\phi^{\max} > 0$; otherwise the delay upper-bound is zero. By [[48], Proposition 7], we obtain $\alpha^{\downarrow}_{\mathrm{reseq}}(k) \geq \alpha^{\downarrow}(k) - V$. Therefore, the delay is upper-bounded by $\theta = \max_{k\in\mathbb{N}}\left\{k\phi^{\max} - \alpha^{\downarrow}(k) + V\right\}$ for nonzero processing time, i.e., $\phi^{\max} > 0$.

We can see that the delay lower bound is $\phi^{\min}$ as minimum processing time for a packet. This gives the jitter $V_{\mathrm{SSQ}} = \theta - \phi^{\min}$. By summing the bounds from A to Z and the single-server FIFO queue, we obtain the bounds in the statement of the theorem.

Lemma 5. *Consider a head-of-line damper shown in Fig. 15. Then, this system can be abstracted as a re-sequencing damper with tolerances $(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}})$ followed by a single-server FIFO queue with service time in range $[\phi^{\min}, \phi^{\max}]$.*

Proof. We use the notation in Fig. 15. Let E be the sequence of actual eligibility times at the head-of-line damper and $\tilde{E}$ the sequence of theoretical eligibility times. By the discussion

that follows (9) and by Lemma 2, there exist sequences $\bar{E}$ and ϕ such that, for every n:

$$\begin{aligned} \phi_n &\in [\phi^{\min}, \phi^{\max}], \\ \tilde{E}_n - \Delta^{\mathrm{L}} \leq & \bar{E}_n \leq \tilde{E}_n + \Delta^{\mathrm{U}}, \\ E_n &= \max(\bar{E}_n, E_{n-1}) + \phi_n. \end{aligned} \tag{65}$$

Let us construct a re-sequencing damper with tolerances $(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}})$ and sequence of actual eligibility times Z such that

$$\begin{aligned} \tilde{E}_n - \Delta^{\mathrm{L}} \leq \bar{E}_n \leq \tilde{E}_n + \Delta^{\mathrm{U}}, \\ Z_1 = \bar{E}_1, \quad Z_n = \max\left\{\bar{E}_n, Z_{n-1}\right\}. \end{aligned} \tag{66}$$

Now consider a single-server FIFO queue with sequence of service times equal to ϕ and input sequence Z. Then, the output sequence from the FIFO queue, O, is

$$O_1 = Z_1 + \phi_1, O_n = \max(O_{n-1}, Z_n) + \phi_n; n \geq 2. \tag{67}$$

We now show by induction that $O_n = E_n$ for every $n \geq 1$. This holds for $n = 1$. Assume that it holds for $n-1$. Observe first that $Z_{n-1} \leq O_{n-1}$ (because $\phi_n \geq 0$) and therefore, by the induction hypothesis,

$$Z_{n-1} \leq E_{n-1}. \tag{68}$$

By (67) and again the induction hypothesis:

$$O_n = \max(E_{n-1}, Z_n) + \phi_n. \tag{69}$$

By (66):

$$\begin{aligned} O_n &= \max(E_{n-1}, \bar{E}_n, Z_{n-1}) + \phi_n \quad (70) \\ &= \max(E_{n-1}, \bar{E}_n) + \phi_n, \quad (71) \end{aligned}$$

because of (68). It follows from (65) that $O_n = E_n$. □

Lemma 6. *Consider a flow with per-packet arrival curve α that enters a single-server FIFO queue. Suppose that a head of line packet n has a processing time $\phi_n \in \left[\phi^{\min}, \phi^{\max}\right]$. Then a delay bound of the flow θ is:*

$$\theta = \max_{i \in \mathbb{N}} \left\{ i\phi^{\max} - \alpha^{\downarrow}(i) \right\}. \tag{72}$$

Proof. Let us call I_n and O_n as arrival and departure times of packet n. By Lemma 7, we have:

$$O_n = \max_{m \leq n} \left\{ I_m + \sum_{i=m}^{n} \phi_i \right\}. \tag{73}$$

We subtract I_n from both sides:

$$\begin{aligned} O_n - I_n &= \max_{m \leq n} \left\{ I_m + \sum_{i=m}^{n} \phi_i \right\} - I_n \\ &= \max_{m \leq n} \left\{ \sum_{i=m}^{n} \phi_i - (I_n - I_m) \right\}. \end{aligned} \tag{74}$$

By [18, Section III.E], we have $I_n - I_m \geq \alpha^{\downarrow}(n - m + 1)$; therefore,

$$O_n - I_n \leq \max_{m \leq n} \left\{ \sum_{i=m}^{n} \phi_i - \alpha^{\downarrow}(n - m + 1) \right\}. \tag{75}$$

Since $\phi_i \leq \phi^{\max}$:

$$\begin{aligned} O_n - I_n &\leq \max_{m \leq n} \left\{ (m - n + 1)\phi^{\max} - \alpha^{\downarrow}(n - m + 1) \right\} \\ &\leq \max_{i \in \mathbb{N}} \left\{ i\phi^{\max} - \alpha^{\downarrow}(i) \right\} = \theta. \end{aligned} \tag{76}$$

□

Lemma 7. *Consider a single-server FIFO queue. A packet n arrives at time I_n and the service time is ϕ_n when it is at the head of the queue. Then, the departure time of packet n is O_n and computed as:*

$$O_n = \max_{m \leq n} \left\{ I_m + \sum_{i=m}^{n} \phi_i \right\}. \tag{77}$$

Proof. Since we have for a single-server FIFO queue:

$$O_1 = I_1 + \phi_1, \quad O_n = \max\left(I_n, O_{n-1}\right) + \phi_n, \tag{78}$$

by Lemma 1 the statement is proven. □

F. Proof of Theorem 5

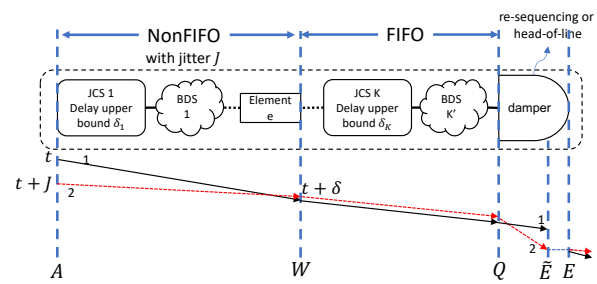

Fig. 16: The notations used in the proof of Theorem 5.

Consider Fig. 16 where A is used to denote the arrival times to JCS 1, W the departure times from element e, Q the arrival times to the damper, $\tilde{E}$ and E respectively the theoretical and actual eligibility times at the damper. Now for packets m, n : $m < n$, since from output of element e to the input of the damper is FIFO, we have $W_m \leq W_n$. Then, as the jitter from JCS 1 to element e is bounded by J, we have:

$$\begin{aligned} &(W_n - A_n) - (W_m - A_m) \leq J \\ &\text{thus } A_m - A_n \leq J + W_m - W_n \leq J \\ &\text{thus } A_n \geq A_m - J. \end{aligned} \tag{79}$$

Now by (5), we have:

$$\begin{aligned} \tilde{E}_n - \Delta^{\mathrm{L}} \leq \bar{E}_n \leq \tilde{E}_n + \Delta^{\mathrm{U}}, \\ E_1 = \bar{E}_1, \quad E_n = \max\left\{\bar{E}_n, E_{n-1}\right\}. \end{aligned} \tag{80}$$

By definition, the re-sequencing damper behaves as a damper with tolerances $(\Delta^{\mathrm{L}}, \Delta^{\mathrm{U}})$ followed by a re-sequencing buffer, where $\bar{E}$ is the output of the damper with tolerance and E is the output of the re-sequencing buffer. Now, let n be fixed and define packet index u as

$$u = \max\left\{ k \leq n | \bar{E}_k = \max_{j \leq n} \left\{ \bar{E}_j \right\} \right\}. \tag{81}$$

Then, we have $E_n - A_n = \bar{E}_u - A_n$. Combining with (79) for packets u and n, we obtain:

$$E_n - A_n \leq \bar{E}_u - A_u + J. \tag{82}$$

Since $\bar{E}$ is the output of the damper with tolerance, by Theorem 1, $\bar{E}_u - A_u \leq \overline{D}$; hence $E_n - A_n \leq \overline{D} + J$, which proves the delay upper bound. By (80) and Theorem 1, we have:

$$E_n - A_n \geq \bar{E}_n - A_n \geq \underline{D}, \tag{83}$$

which proves the delay lower bound for this case. Since the delay lower-bound is not changed, and the upper-bound is increased by J, hence the jitter bound is increased by J.

Proof of tightness. The tightness scenario for delay lower-bound is exactly the same as tightness scenario in Theorem 1 where a single packet in isolation reaches the delay lower-bound $\underline{D}$.

For the delay upper-bound and jitter bound tightness, consider two packets 1 and 2 as shown in Fig 16 that arrive at times t and $t + J$ in TAI. Assume every local clock (of JCS or damper) $\mathcal{H}_i$ is adversarial and faster than TAI such that for any delay measurement d, we have:

$$d^{\mathcal{H}_{\text{TAI}}} = \min\left(\rho d^{\mathcal{H}_i} + \eta, d^{\mathcal{H}_i} + 2\omega\right).$$

Let us call the worst-case delay, in TAI, from input of JCS 1 to the output of e, as δ. Suppose that packets 1 and 2 experience delays of δ and $\delta - J$, in TAI, to leave element e, i.e., $W_1 = W_2 = t + \delta$, and packet 2 arrives just before packet 1. Also, both experience the same delay from output of element e to the input of the damper while packet 2 is still prior to packet 1 due to the FIFO assumption. Since packet 1 arrives after packet 2, it is released after packet 2 becomes eligible (even if its theoretical eligibility time has passed).

Now, assume packet 2 experiences a delay, in TAI, equal to $\overline{D}$ from A to E, i.e., $E_2 = A_2 + \overline{D} = t + J + \overline{D}$ (the packet that reaches the upper-bound in tightness scenario of Theorem 1). Therefore, packet 1 is released after packet 2, i.e., $E_1 = E_2 = t + J + \overline{D}$. Hence, the delay of packet 1 from A to E is:

$$E_1 - A_1 = (t + J + \overline{D}) - (t) = J + \overline{D}, \tag{84}$$

that is equal to the delay upper-bound of the theorem statement.

Now, we verify the assumptions;

1) The jitter from JCS 1 to the output of e is not larger that J: The delay of packet 1 and packet 2 are respectively δ and $\delta - J$ in TAI, and therefore the jitter is J.

2) The FIFO constraint of the damper is not violated: Packet 2 arrives before packet 1, $Q_2 \leq Q_1$, and also leaves before is $E_2 \leq E_1$.

Hence, we showed an execution trace that with packet 2 experiencing a delay of $\overline{D}$, packet 1 experiences a delay of $\overline{D} + J$. Since there execution traces where in one, a packet reaches the lower-bound of Theorem 1 and in another one, a packet reaches the delay upper-bound of Theorem 1 plus J, we have that the jitter Theorem 1 is increased by J.

G. Proof of Theorem 6

Consider Fig. 16 where A is used to denote the sequence of arrival times to JCS 1, W the departure times from element e, Q the arrival times to the damper, $\tilde{E}$ and E respectively the theoretical and actual eligibility times at the damper. By Lemma 5, we abstract it as a re-sequencing damper followed by a single-server FIFO queue. Let Z denote the sequence of departure times from the re-sequencing damper; then, by Theorem 5, for a packet n, we have:

$$\underline{D} \leq Z_n - A_n \leq \overline{D} + J, \tag{85}$$

and the jitter from A to Z is $V + J$. As a result, by [18, Lemma 1], an arrival curve at the output of the re-sequencing damper (input of the single-server FIFO queue) is $\alpha_{\text{reseq}} = \alpha(t+V+J)$. Then by Lemma 6 for nonzero processing time:

$$\begin{aligned} E_n - Z_n &\leq \max_{k\in\mathbb{N}} \left\{k\phi^{\max} - \alpha^{\downarrow}_{\text{reseq}}(k)\right\} \\ &\leq \max_{k\in\mathbb{N}} \left\{k\phi^{\max} - \alpha^{\downarrow}(k) + V + J\right\} = \theta + J, \end{aligned} \tag{86}$$

where θ is defined in (28). Finally, by (85), we have,

$$\begin{aligned} E_n - A_n &= (E_n - Z_n) + (Z_n - A_n) \\ &\leq \overline{D} + J + (\theta + J)1_{\{\phi^{\max}>0\}}, \end{aligned} \tag{87}$$

which proves the delay upper bound. Note that by Theorem 4, an upper-bound on the delay is $\overline{D} + \theta 1_{\{\phi^{\max}>0\}}$.

Using minimum processing time and (85), we have:

$$\begin{aligned} E_n - A_n &= (E_n - Z_n) + (Z_n - A_n) \\ &\geq \phi^{\min} + \underline{D}, \end{aligned} \tag{88}$$

which proves the delay lower bound. Since the delay lower-bound is not changed, and the upper-bound is increased by $J + J1_{\{\phi^{\max}>0\}}$, the jitter bound is increased by $J + J1_{\{\phi^{\max}>0\}}$.